PVT-ROBUST ULTRA-LOW-JITER CLOCK MULTIPLIERS USING AN INJECTION-LOCKING TECHNIQUE

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Abstract

This thesis presents process-voltage-temperature (PVT)-robust ultra-low-jitter clock multipliers using an injection-locking technique. First, an injection-locked clock multiplier (ILCM) using a two-phase PVT-calibrator is proposed. The proposed PVT-calibration technique is based on the dual-loop architecture which consists of a main-voltage-controlled oscillator (VCO) and a replica-VCO. While the main-VCO is injection-locked and generates the precise target frequency, the real-time frequency variation of the replica-VCO can be monitored by the PVT-calibrator which adjusts the control voltage shared by the two identical VCOs. Using the two-phase calibration technique, the tradeoff between the calibration resolution and the lock time was removed. The proposed ILCM, fabricated in the 65-nm CMOS process, generated five different reference frequencies, i.e., 19.2, 28.8, 48.0, 57.6, and 96.0 MHz with a 19.2 MHz external clock. When injection-locked, the integrated jitter from 1 kHz to 10 MHz of the 96-MHz signal was 1.69 ps. The proposed PVT-calibrator restricted the phase noise degradation over the temperature range of 30 to 80 ℃ to less than 0.5 dB. Second, a fractional-resolution ILCM using a delay-locked-loop (DLL)-based PVT-calibrator is proposed. In this architecture, the ring-type VCO and the voltage-controlled delay line (VCDL) of the DLL consist of identical delay cells, and they share the same control voltage. Thus, by changing the ratio between the numbers of stages of the VCDL and the VCO, the frequency of the VCO can be calibrated at a target frequency, a non-integer times the reference frequency. The proposed ILCM, designed in the 65-nm CMOS process, generated output frequencies that range from 1.2 to 2.0 GHz with a frequency resolution of 40 MHz with a 400-MHz reference clock. When injection-locked, the integrated jitter from 1 kHz to 40 MHz of the 1.6-GHz signal was 440 fs. The proposed DLL-based PVT-calibrator restricted the degradations of phase noise and jitter over the temperature and the supply variations to less than 0.7 dB and 20%, respectively. Both architectures presented in this thesis can overcome real-time frequency drifts as well as static process variations; thus, excellent jitter performance can be sustained during any environmental variations.

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I. Introduction

As the demand for low-jitter clock multipliers with small areas and low power consumptions increases, sub-harmonic injection-locked clock multipliers (ILCMs) are now receiving a great deal of attention. To date, the most extensively used architectures for generating high-performance clocks have been based on a phase-locked-loop (PLL) with an *LC*-oscillator, but their low level of integration has been a bottleneck in the effort to reduce the cost of implementation. Recently, new architectures based on a subharmonic ILCM [1]–[18] have emerged as alternatives to conventional PLL-based clock multipliers. Those architectures possess the intrinsic mechanism of phase realignment by the reference clock. Therefore, they can generate precise clock signals with excellent jitter performance without the need for an external loop, even though they use a ring-type oscillator that provides poor spectral purity. Nevertheless, conventional sub-harmonic ILCMs have an inherent disadvantage, i.e., the coarse resolution of achievable output frequencies. The frequency resolution of conventional ILCMs is equal to the reference frequency, because they generate output frequencies that are integer multiples of the reference frequency. Also, ILCMs have another critical problem, i.e., injection locking can occur only when the difference between the frequency of the free-running voltage-controlled oscillator (VCO) and the target frequency is sufficiently small within the lock range. Generally, the lock range is much narrower than the amount of the possible change in the frequency of a ring-VCO due to process-voltage-temperature (PVT) variations. If the frequency difference is out of the lock range, the injection-locked oscillator will fail in the lock acquisition [1]. Even if the frequency difference between the free-running frequency of the VCO and the target frequency is smaller than the lock-range, a large frequency deviation might result in degradation of the jitter performance. To overcome this problem, a practical ILCM must be equipped with a dedicated PVT-calibrator that can reduce the frequency difference. The most popular calibration method for an ILCM is to place the injection-locked VCO inside a PLL [2]–[4], [8]–[10]. However, the PLL-based calibration method is not a complete solution. While it can correct the static frequency change due to process corners, it cannot correct the instantaneous frequency drift caused by temperature or voltage variations [11]–[15], [19]. This is because the VCO generates a fixed output frequency when it is injection-locked, and the drift of the free-running frequency of the VCO cannot be detected by the PLL. Thus, there could be significant degradation of jitter, depending on the magnitude of the frequency's drift. Moreover, if the deviation of the free-running frequency of the VCO becomes larger than the lock range, the injection lock can even be released. Recently, there have been efforts to calibrate the real-time frequency drift as well as the static frequency deviation, but there still exist unsolved problems.

In this thesis, PVT-robust ultra-low-jitter clock multipliers using an injection-locking technique are presented [19], [20]. Using a real-time PVT-calibrator, the proposed ILCMs can overcome major problems that have prevented practical use of conventional ILCMs in commercial ICs.

First, an ILCM using a two-phase PVT-calibrator is proposed for use in a PLL. The proposed PVT-calibration technique is based on the dual-loop architecture which consists of a main-VCO and a replica-VCO. While the main-VCO is injection-locked and generates the precise target frequency, the real-time frequency variation of the replica-VCO can be monitored by the PVT-calibrator which adjusts the control voltage shared by the two identical VCOs. Using the two-phase calibration technique, the tradeoff between the calibration resolution and the lock time was removed.

Second, a fractional-resolution ILCM using a delay-locked-loop (DLL)-based PVT-calibrator is proposed. In this work, the injection-locked ring-VCO and the voltage-controlled delay line (VCDL) of a DLL consist of identical delay cells, and they share the same control voltage, V_{CONT}. As the DLL keeps adjusting V_{CONT} to maintain the constant delay of the delay cells in the VCDL, the injection-locked VCO, which consists of the same delay cells, can also correct the frequency drift by sharing V_{CONT}. In addition, by rotationally switching the injection point of the multistage ring-VCO as in [9], the ILCM achieved a fractional resolution that was one-tenth of the reference frequency. By changing the ratio between the numbers of the stages of the VCDL and the VCO, the proposed DLL-based PVT-calibrator can easily tune the VCO frequency to a target frequency, i.e., a noninteger times the reference frequency.

In both architectures, good jitter performance can be sustained even with real-time environmental variations. Moreover, the proposed ILCMs are free from the injection-timing issue of conventional PLL-based injection-locked architectures, since the VCO is not locked by the loop [13].

This thesis is organized as follows: Section II provides background information on clock multipliers, and conventional PVT calibration techniques for ILCMs. In Section III and IV, the proposed PVT calibrators are introduced. Experimental results are presented in Section V, and the conclusion is presented in Section VI.

II. Background

2.1. PLL-based clock multiplier

2.1.1. Overview of PLL

The most extensively used architectures for generating high-performance clocks are based on a PLL. A basic PLL consists of a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), VCO, and a divide-by-*N* frequency divider as shown in Figure 1. f_{REF} and f_{OUT} represent the reference frequency and the output frequency, respectively. In the PLL, the PFD detects phase or frequency differences between its two inputs. According to the output of the PFD, the CP charges or discharges the loop filter to adjust the control voltage of the VCO. The output frequency of the VCO can be represented as,

$$\omega_{VCO} = \omega_0 + K_{VCO} \cdot V_{CONT}, \tag{1}$$

where K_{VCO} is the gain of the VCO in rad/s/V, and V_{CONT} is the control voltage of the VCO. Since a PLL is a negative feedback system, the frequency error between f_{REF} and f_{OUT}/N will be forced to zero in the steady state. In other words, the output frequency, f_{OUT}, can be expressed as the following equation in the locked condition.

$$f_{VCO} = N \cdot f_{REF}, \tag{2}$$

Multiple output frequencies can be obtained from one reference frequency by changing *N*. Since the available output frequencies are only integer multiples of the reference frequency, a PLL represented in Figure 1 is called an integer-*N* PLL. In this architecture, the frequency resolution of the output clock is restricted to f_{REF}, which is the major limitation of integer-*N* PLLs.

In general PLL-based clock multipliers, an *LC*-VCO is used to satisfy stringent phase noise requirements. However, their low level of integration has been a bottleneck in the effort to reduce the cost of implementation. PLL-based clock multipliers also require a bulky loop filter for the loop stability, since the system of a PLL has two poles at the origin.

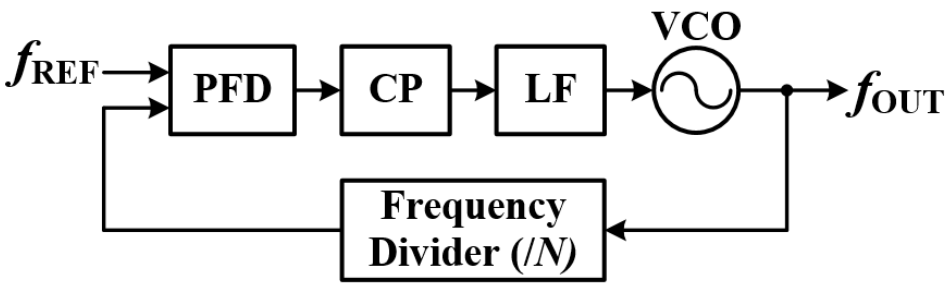


Figure 1. Block diagram of phase-locked loop.

2.1.2. Linear model of PLL

Figure 2 shows the model of conventional integer-*N* PLLs which can generate integer multiples of the reference frequency. ϕ_{REF}, ϕ_{VCO}, and ϕ_{OUT} represent the excess phase of the reference, the VCO and the output signal, respectively. In reality, the combination of the PFD and CP (PFD/CP) operates in discrete-time. The PFD produces pulses whose width is proportional to the phase difference in every reference period, and the CP charges or discharges the loop filter with a constant current, I_{CP}. However, to simplify the analysis, the PFD/CP is approximated as a linear, continuous-time system. In the continuous-time model, the output current of the PFD/CP is proportional to the phase difference of the inputs. Because of this, the loop bandwidth of the PLL should be less than 1/20 of the reference frequency in order to ensure the accuracy of the model. Using the model in Figure 2, the loop gain of the PLL can be calculated as follows,

$$T(s) = \frac{I_{CP}}{2\pi} \cdot F(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} \tag{3}$$

where F(s) is the transfer function of the LF. The transfer function of the VCO has a pole at the origin, since the phase is computed as the integration of the frequency. Therefore, the transfer function of the LF, $F(s)$, should be carefully designed to provide enough phase margin as well as a sufficient attenuation of ripples in the control voltage. The 2nd order loop filter for a 3rd order PLL is shown in Figure 3. Using the second order loop filter in Figure 3, the loop gain can be calculated as

$$T(s) = \frac{I_{CP} K_{VCO}}{2\pi (C_1 + C_2) N} \frac{1}{s^2} \cdot \frac{1 + sR_1C_1}{1 + \frac{R_1C_1C_2}{C_1 + C_2} s} = K_{PLL} \cdot \frac{1}{s^2} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}, \tag{4}$$

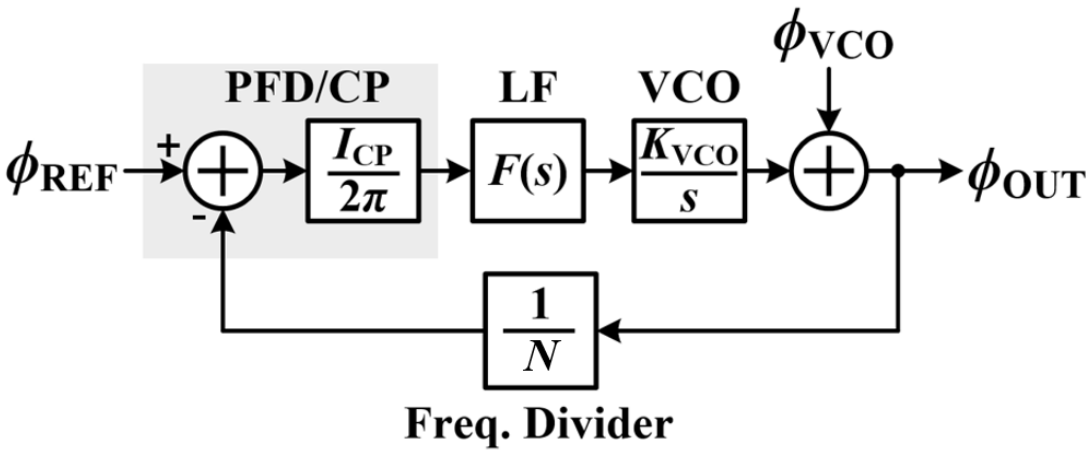


Figure 2. Linear model of a PLL.

where K_{PLL}, ω_z and ω_p can be represented as follows.

$$K_{PLL} = \frac{I_{CP} K_{VCO}}{2\pi (C_1 + C_2) N} \tag{5}$$

$$\omega_z = \frac{1}{R_1 C_1} \tag{6}$$

$$\omega_p = \frac{C_1 + C_2}{R_1 C_1 C_2} \tag{7}$$

Using (4), transfer functions to ϕ_{OUT} from ϕ_{REF} and ϕ_{VCO} can be computed as

$$\frac{\phi_{OUT}}{\phi_{REF}}(s) = \frac{T(s) \cdot N}{1 + T(s)} = \frac{K_{PLL} N \cdot \frac{1}{s^2} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p}}{1 + K_{PLL} \cdot \frac{1}{s^2} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p}} = \frac{K_{PLL} N \cdot (1 + s/\omega_z)}{s^2 (1 + s/\omega_p) + K_{PLL} (1 + s/\omega_z)}, \tag{8}$$

and $$\frac{\phi_{OUT}}{\phi_{VCO}}(s) = \frac{1}{1 + T(s)} = \frac{1}{1 + K_{PLL} \cdot \frac{1}{s^2} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p}} = \frac{s^2 (1 + s/\omega_p)}{s^2 (1 + s/\omega_p) + K_{PLL} (1 + s/\omega_z)}, \tag{9}$$

respectively. (8) shows a low-pass characteristic, and has a DC gain of *N*, while (9) has a high-pass characteristic.

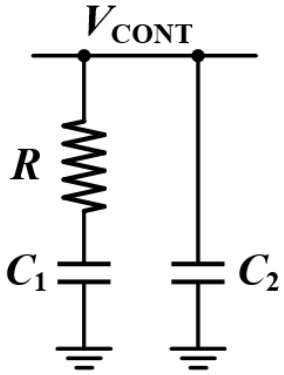


Figure 3. Second order loop filter for a third order PLL

2.1.3. ΔΣ PLL

In order to achieve a finer frequency resolution in an integer-*N* PLL, the reference frequency should be scaled down. Also, the value of *N* should be proportionally increased to maintain the constant output frequency. However, reducing the reference frequency would result in problems. First, the increased *N* would result in higher in-band phase noise, because noise transfer functions from loop building blocks such as a PD and a CP are proportional to *N*. In other words, in-band noise is amplified by the factor of *N* at the output of the PLL. Even though the decreased operating frequency partially cancels out the effect of noise amplification, the overall noise contribution from loop building blocks still includes the term, $10 \cdot \log N$, in dB. Second, a small reference frequency would limit the bandwidth, and cause a longer settling time. In order to solve these tradeoffs of an integer-*N* PLL, a fractional-*N* PLL can be used.

A delta-sigma PLL (ΔΣ PLL) or a fractional-*N* PLL is a PLL that adopts a delta-sigma modulator (DSM) as shown in Figure 4, to overcome the limitation of the frequency resolution in integer-*N* PLLs. A basic DSM generates a bit stream whose average is the desired value between 0 and 1, and the quantization noise at the output of the DSM is high-pass-shaped. By toggling the division ratio of the frequency divider between *N* and *N*+1 using the DSM, the average division ratio can be a fractional number, whose integer part is equal to *N*. As a result, the achievable frequency resolution becomes fractional multiples of the reference frequency, and a fine frequency resolution can be achieved from the fixed reference frequency by using a DSM. The quantization noise of the DSM can be suppressed by low-pass filtering of the PLL, since the quantization noise has a high-pass spectrum.

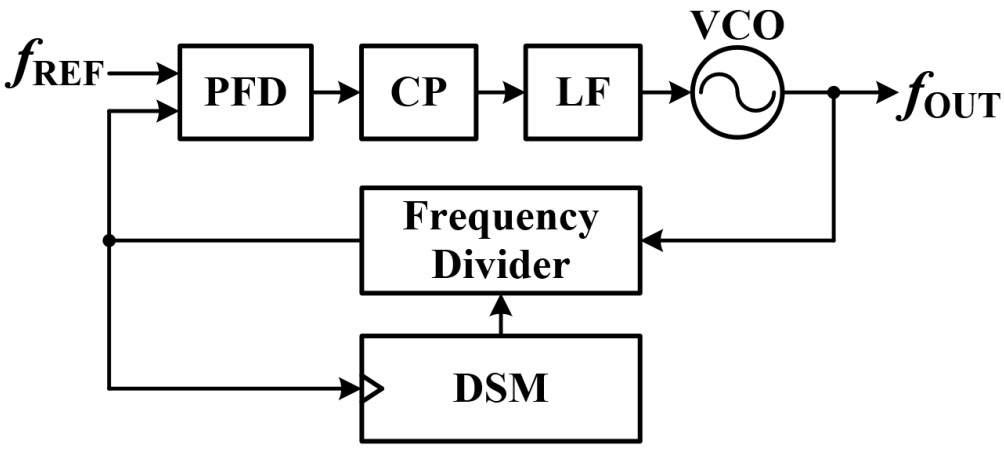


Figure 4. Block diagram of a delta-sigma PLL.

2.2. DLL-based clock multiplier

Figure 5 shows the block diagram of a DLL-based clock multiplier. The conventional DLL consists of a phase detector (PD), a CP, a LF, and a VCDL with N delay cells. Compared to a PLL, a DLL uses a PD and VCDL instead of a PFD and VCO. The basic operation of a DLL is similar to that of a PLL. When the DLL is locked, the total delay of the VCDL becomes equal to the period of the reference clock, T_{REF}, since the phase difference between the reference clock and the output of the VCDL becomes zero in the locked condition. Since the VCDL consists of N identical delay cells, the delay of one delay cell is equal to T_{REF}/N, if mismatches between delay cells and other non-idealities are neglected. Therefore, the outputs of delay cells can be utilized to generate integer multiples of the reference frequency.

DLL-based clock multipliers have several advantages over PLL-based architectures. First, the feedback system of a DLL is inherently stable, because the system of a DLL has only one pole at the origin. Since the stability issue is relaxed, the bandwidth can be extended to achieve a shorter settling time. Also, jitter is not accumulated from cycle to cycle, since the reference signal cleans up the accumulate jitter in every reference period. Therefore, DLL-based clock multipliers can achieve a good jitter performance without using an *LC*-VCO which occupies a large silicon area.

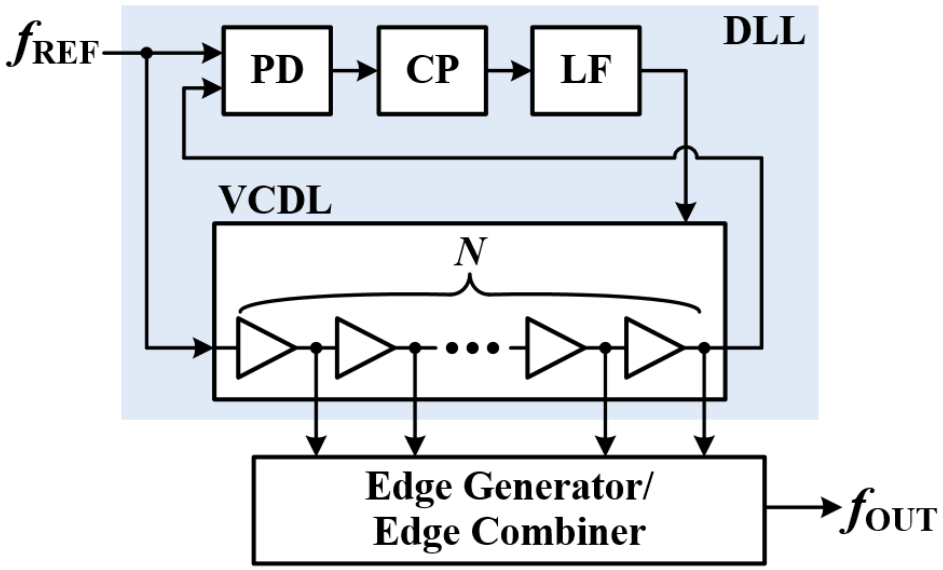


Figure 5. Block diagram of DLL-based clock multiplier.

2.3. Injection-locked clock multiplier

2.3.1. Overview of ILCM

Figure 6 shows a subharmonic injection-locked VCO. The injection signal is generated from the reference clock by a pulse generator. When the free-running frequency of the VCO is close to the N^{th} harmonic of the reference frequency, the output frequency, f_{OUT}, becomes N times the reference frequency, f_{REF}, in the locked condition. Since the injection signal periodically realigns the phase of the VCO, the phase noise accumulation can be greatly suppressed. The noise model of the injection-locked VCO is shown in Figure 7. The noise transfer functions in the noise model, H_{INJ} and H_{UP} can be represented as

$$H_{INJ}(j\omega) = 1 - \frac{\beta \cdot e^{-j\omega T_{REF}/2}}{1+(\beta-1)e^{-j\omega T_{REF}}} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}, \tag{10}$$

$$\text{and} \quad H_{UP}(j\omega) = \frac{N \cdot \beta \cdot e^{-j\omega T_{REF}/2}}{1+(\beta-1)e^{-j\omega T_{REF}}} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}, \tag{11}$$

where β is the phase realignment factor that indicates how completely the phase error can be suppressed by the reference clock [2], [3]. As shown in Figure 8, β is defined as $-\theta_r/\theta_e$, where θ_r is the phase shift due to the injection and θ_e is the phase error between the VCO output and the reference clock just before the injection. Therefore, β ranges from 0 to 1, where $\beta = 0$ means no injection, and $\beta = 1$ means complete phase realignment by the injection. The value of β is affected by not only the strength and the pulse width of the injected signal, but also the difference between the free-running frequency of the VCO and the target frequency.

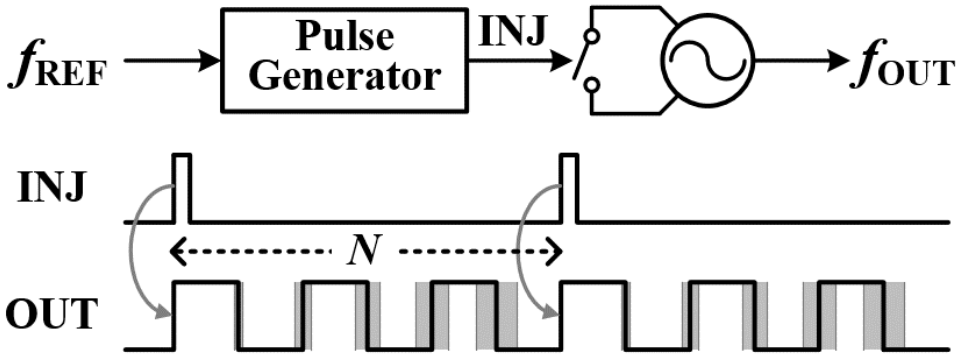


Figure 6. Block diagram of injection-locked VCO.

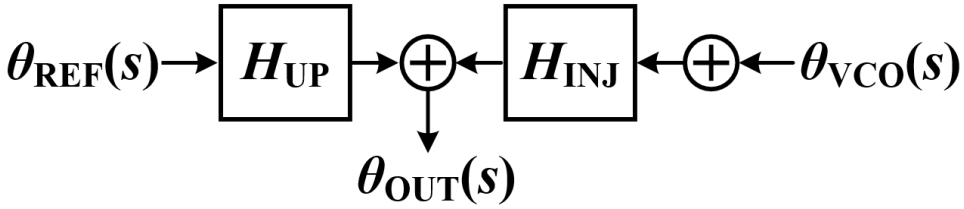


Figure 7. Noise model of injection-locked VCO.

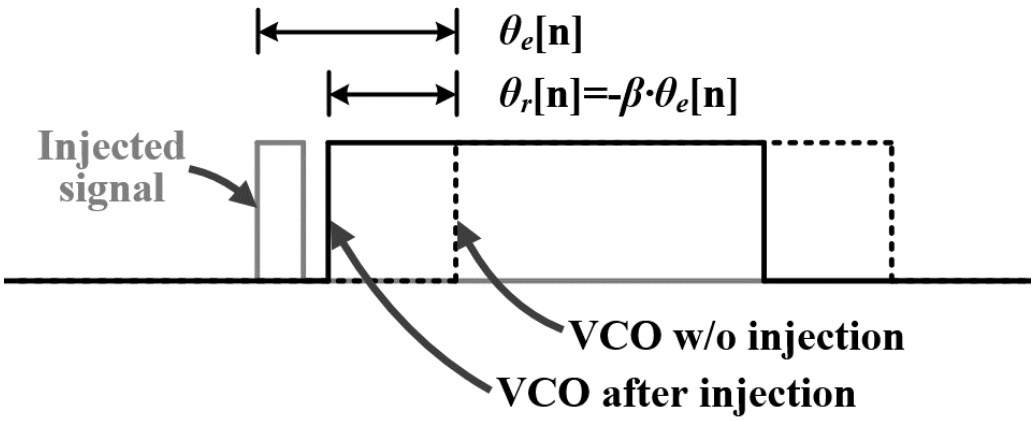


Figure 8. Phase realignment due to injection.

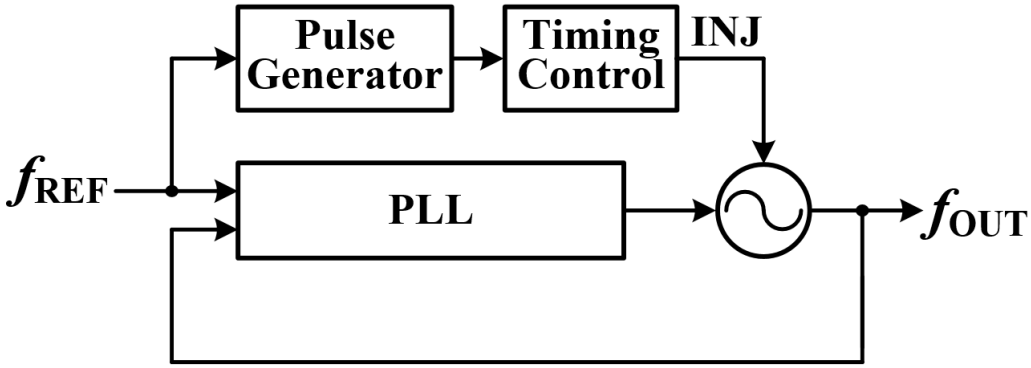
2.3.2. Conventional PVT-calibrators for ILCMs

In order to take the full advantage of injection-locking on the jitter performance, the difference between the frequency of the free-running VCO and the target frequency must be tightly controlled. Even if the frequency difference between the free-running frequency of the VCO and the target frequency is smaller than the lock-range, a large frequency deviation might result in degradation of the jitter performance. Recently, many efforts have been made to design on-chip PVT-calibrators, and their architectures can be categorized as shown in Figure 9.

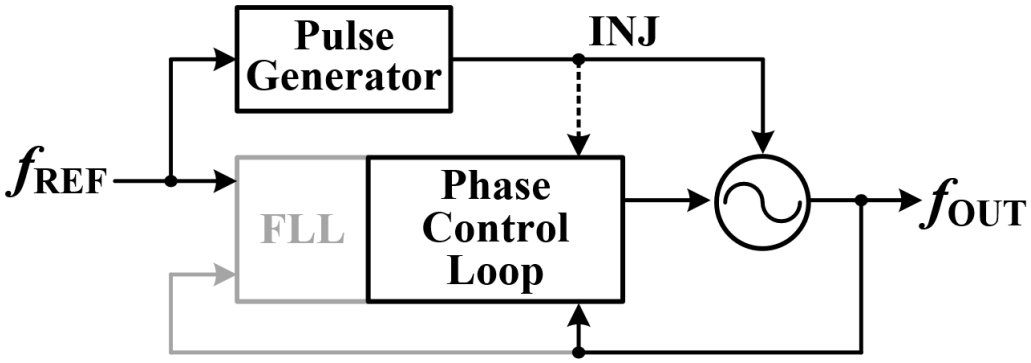
One of the most extensively used on-chip calibration architectures is to utilize a PLL to correct the VCO frequency. In this method, a single VCO is enclosed by a single PLL loop and reference pulses are injected to the VCO. This method is generally vulnerable to the timing issue, caused by two independent phase-corrections through the injection-path and the PLL-path [12], [13]. Therefore, recent architectures [8], [9], [10] include an additional control circuit that adjusts the timing of the injection, as shown in Figure 9(a). However, as mentioned in Section I, these PLL-based calibrators with a single VCO have a fundamental problem, i.e., they cannot detect any real-time frequency drifts due to temperature or voltage variations while they can overcome the static process variations [12], [13]. This is because the injection pulse keeps resetting the instantaneous phase-error in every reference cycle when the VCO is injection-locked. Thus, the PLL cannot detect the real-time frequency drift, which could result in significant degradation of jitter.

To correct instantaneous frequency drifts as well as static frequency deviations, real-time PVT calibrators have been developed using a phase-control loop that can continuously adjust the phase of the VCO signal to be aligned with an injection-pulse [11], [16]–[17], as shown in Figure 9(b). However, since phase-control loops correct only the phase of the VCO signals, they require additional frequency-locked loops (FLLs) at the initial stage of calibration. FLLs are supposed to be turned off during normal operation; thus, these architectures must suffer from a limited-range.

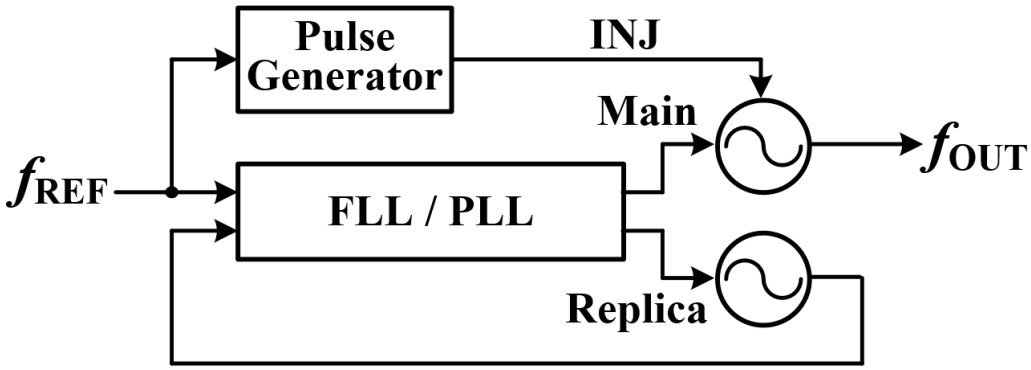
Figure 9(c) shows another real-time PVT-calibration architecture, using a dual-loop and two identical VCOs [12]–[15]. In this method, the main-VCO is injection-locked and generates the precise target frequency, while the PVT-calibrator continuously monitors the real-time frequency variation of the replica-VCO and adjusts the control voltage shared by the two identical VCOs. Since the replica VCO is not injection-locked, the FLL (or PLL) involving the replica VCO can keep detecting the real-time drift of the VCO's frequency. In addition, ILCMs using this calibration method are free from the injection timing issue because the main-VCO is not locked by a loop. However, since the FLL (or PLL) in [12]–[15] consisted of digital circuits, such as counters, digital-to-analog converters (DACs), and digital comparators, a tight tradeoff exists between the frequency switching time and the calibration resolution. Thus, the frequency-switching time required to set the free-running frequency of the VCO sufficiently close to the target frequency must be considerably long.



(a)



(b)



(c)

Figure 9. Conventional PVT-calibrators based on (a) PLL with a timing control; (b) phase-control-loop and (c) dual-loop FLL/PLL.

2.3.3. Fractional injection technique

In conventional subharmonic injection-locked architectures, the injection signal is applied to the fixed node of the VCO. Recently, the fractional injection technique is proposed to enhance the frequency resolution of the injection-locking [9]. By dynamically changing the injection point of a multi-stage ring-VCO, the clock multiplier using the fractional-injection technique can generate the fractional multiples of the reference frequency. The frequency resolution that is achievable from fractional-injection is inversely proportional to the number of stages in the VCO, as shown as follows:

$$f_{RES} = \frac{f_{REF}}{2 \cdot N_{VCO}}, \tag{12}$$

Figure 10 shows an example of the fractional injection technique when N_{VCO} is 2.

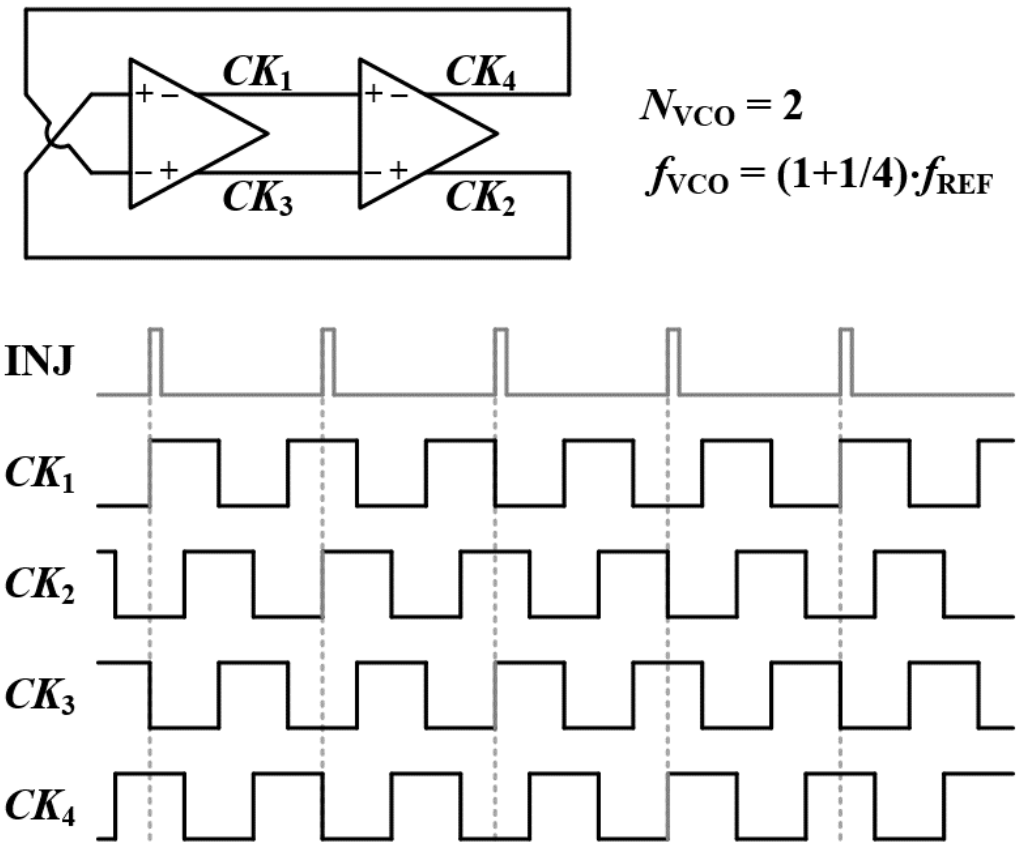


Figure 10. Timing diagram of fractional injection when N_{VCO} = 2.

III. Proposed dual-loop ILCM using a two-phase PVT-calibrator

In this chapter, the dual-loop ILCM using a two-phase PVT-calibrator is presented. This ILCM was used as a reference clock multiplier to reduce the quantization noise in a fractional-*N* PLL. In a fractional-*N* PLL, minimizing the quantization noise is an important issue in satisfying stringent cellular standards. One of the methods of reducing the quantization noise is to increase the reference frequency, because the quantization noise due to the DSM is peaked at $f_{REF}/2$, as shown in Figure 11. Therefore, in order to suppress the quantization noise, the reference frequency of the PLL can be increased by using an ILCM to strengthen the low-pass filtering effect.

The proposed ILCM adopted a PVT-calibrator based on a dual-loop FLL. As discussed earlier, there exists a tight tradeoff between the frequency-acquisition time and the calibration resolution in conventional dual-loop-based PVT-calibrators, as the FLL (or PLL) consists of digital circuits. To address this problem, a two-phase calibration technique was proposed. In the first phase, the calibration resolution of the FLL is coarse. Therefore, it can quickly bring the frequency of the VCO within the lock-range. In the second phase, the calibrator narrows the resolution and starts tracking the real-time frequency drifts over environmental variations. As a result, the proposed ILCM reduces the frequency-switching time, as well as tightly regulating the real-time degradation of jitter.

Figure 12 shows the overall architecture of the proposed ILCM, which consists of a main-VCO, a replica-VCO, a two-phase PVT-calibrator, two pulse generators, a divide-by-*N* frequency divider, and a DAC. f_{XO} and f_{REF} represent the reference frequency of the ILCM and the PLL, respectively, and f_{VCO_M} and f_{VCO_R} represent the frequency of the main-VCO and the replica-VCO, respectively. When the first-phase calibration starts, the PVT-calibrator adjusts the control voltage of the VCO, V_{CONT}, by changing the DAC_CODE to bring f_{VCO_R} close to the target frequency, $N \cdot f_{XO}$. Since the control voltage, V_{CONT}, is shared by the two VCOs, f_{VCO_M} also becomes close to $N \cdot f_{XO}$. When the difference between f_{VCO_M} and $N \cdot f_{XO}$ is sufficiently small within the lock-range, the main-VCO can generate the precise target frequency and the second-phase calibration starts.

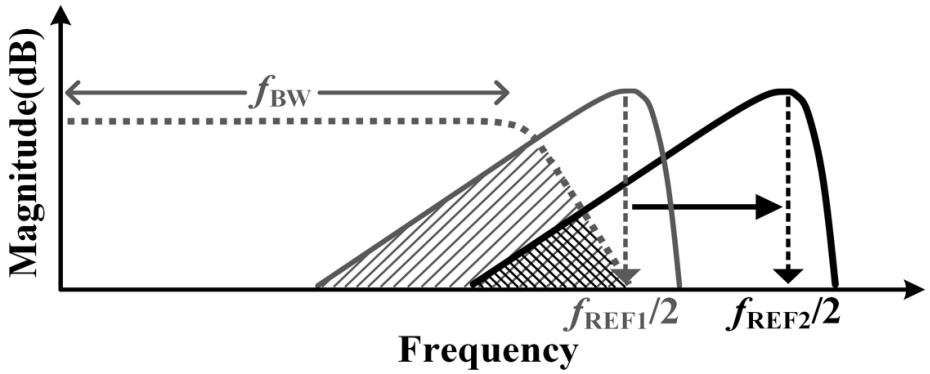


Figure 11. Suppression of the quantization noise when the reference frequency increases.

Figure 13 shows the operation of the two-phase calibration technique. In the first phase, the PVT-calibrator can quickly adjust the control voltage to bring f_{VCO_R} close to $N \cdot f_{XO}$. In the second phase, the calibration resolution is reduced, so the control voltage is finely adjusted. Therefore, the noise degradation of the injection-locked VCO can be tightly restricted.

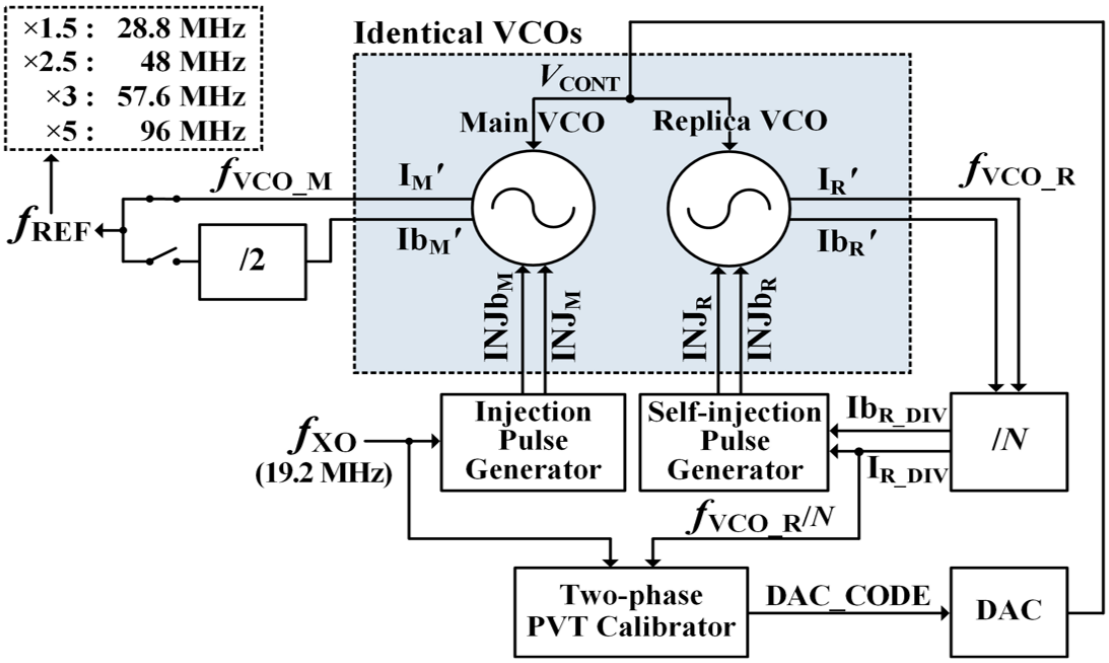


Figure 12. Block diagram of the proposed ILCM.

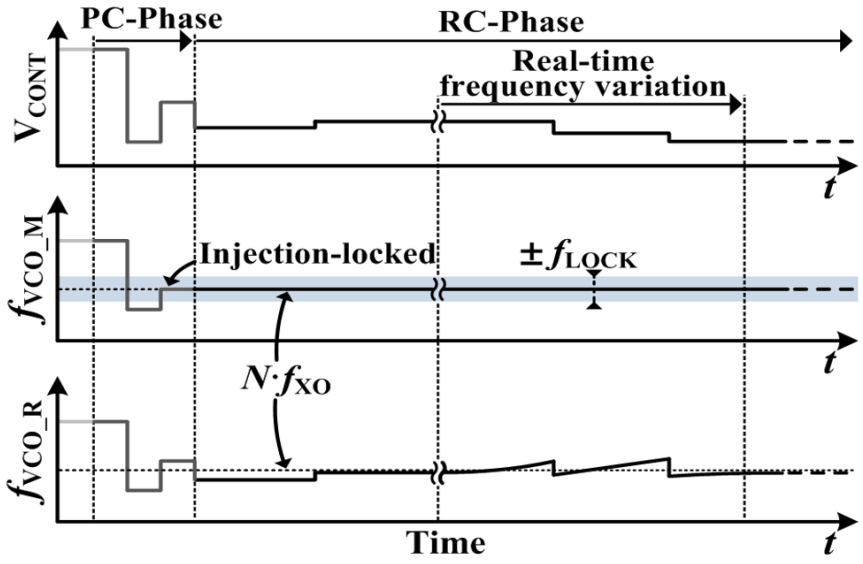


Figure 13. Operation of the two-phase PVT-calibrator.

3.1. Implementation

Figure 14 shows the block diagram of the proposed two-phase PVT-calibrator. First, the normalized frequency of the replica-VCO, f_{VCO_R}/N, enters the calibrator. Then, the k-bit counter counts the rising edges of the signal with f_{VCO_R}/N during T_{WINDOW} to provide the corresponding digital code, VCO_FREQ<k:0>. The window generator consists of an m-bit counter and a divide-by-2 circuit to define T_{WINDOW} as $2^m/f_{XO}$. The subtractor quantifies the difference between f_{VCO_R}/N and f_{XO} as FREQ_DIFF<k:0> by subtracting VCO_FREQ<k:0> from the code designating f_{XO}, TARG_FREQ<k:0> = 2^m. The accumulator adds FREQ_DIFF<k:0> to DAC_CODE<k:0>, to adjust the control voltage. If FREQ_DIFF<k:0> is zero, that calibration phase is completed. In the window generator, the value of m determines the accuracy and the speed of the calibration. In the first phase, m is set to a small value ($m = k - 3$) to achieve the fast calibration. In the second phase, m is set to a high value ($m = k$), and the calibration becomes accurate. Since FREQ_DIFF<k:0> is evaluated by the counter, there exists a frequency error, even when FREQ_DIFF<k:0> is zero. The possible error range can be calculated as

$$\left| \frac{f_{VCO\_R}}{N} - f_{XO} \right| < \frac{1}{T_{WINDOW}} = \frac{f_{XO}}{2^m}. \tag{13}$$

This implies that the value of m must be increased to improve the accuracy of the calibration. However, a higher m inevitably increases the evaluation time as well as the system complexity.

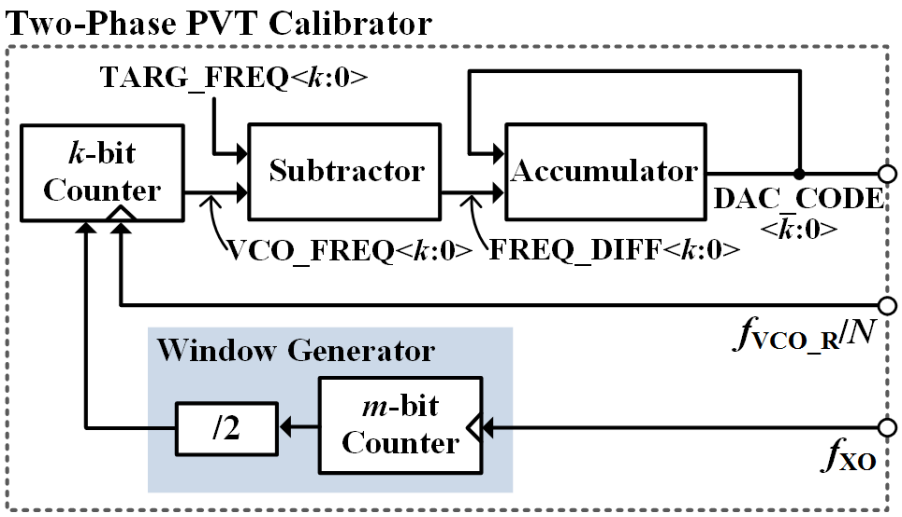


Figure 14. Block diagram of the proposed two-phase PVT-calibrator

The effect of the noise suppression caused by the injection-locked reference clock multiplier was evaluated with a prototype PLL as shown in Figure 15. The PLL consisted of an *LC*-VCO, a PFD, a CP, and a frequency-divider involving a 1-1 multistage-noise-shaping (MASH)-type DSM. The block diagram of the 1-1 MASH-type DSM is shown in Figure 16. The VCO of the ILCM can be locked to either the 3rd or 5th harmonic of the 19.2-MHz frequency. Using a divide-by-2 divider, the clock multiplier can generate five frequencies, i.e., 19.2, 28.8, 48.0, 57.6, and 96.0 MHz.

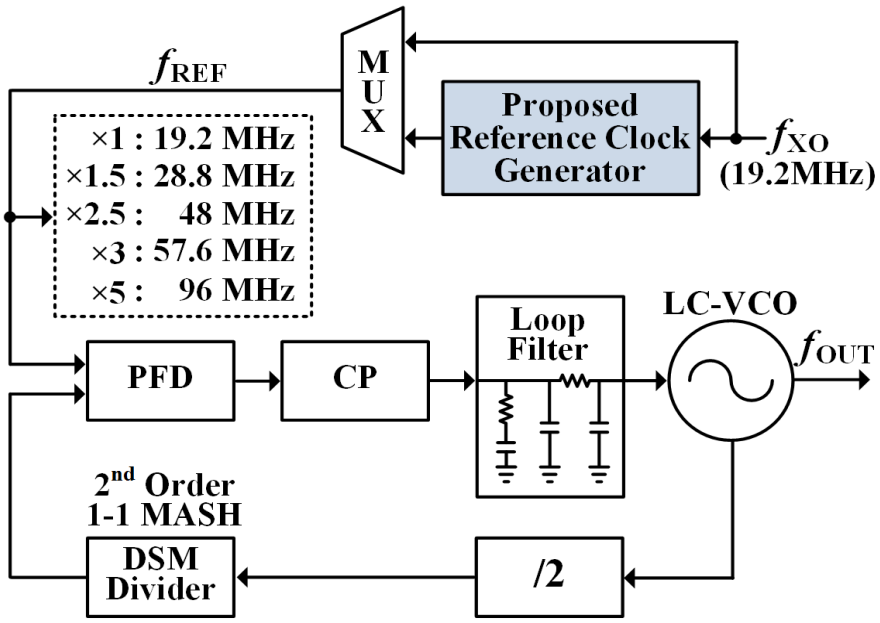


Figure 15. Prototype fractional-*N* PLL with the proposed injection-locked reference clock multiplier.

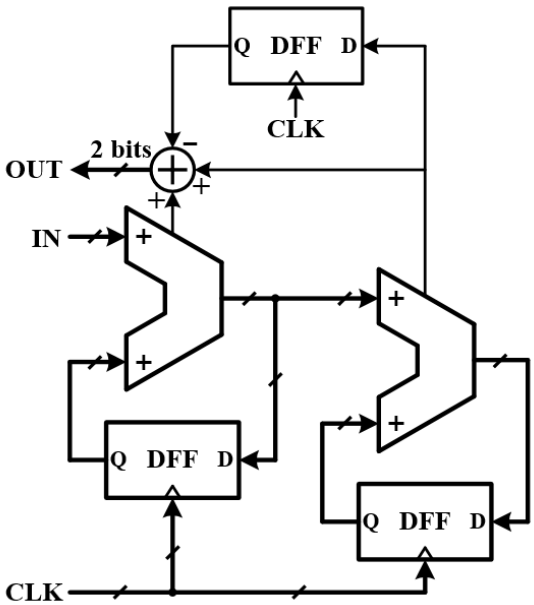


Figure 16. Block diagram of the 1-1 MASH-type DSM.

IV. Proposed fractional-resolution ILCM using a DLL-based PVT-calibrator

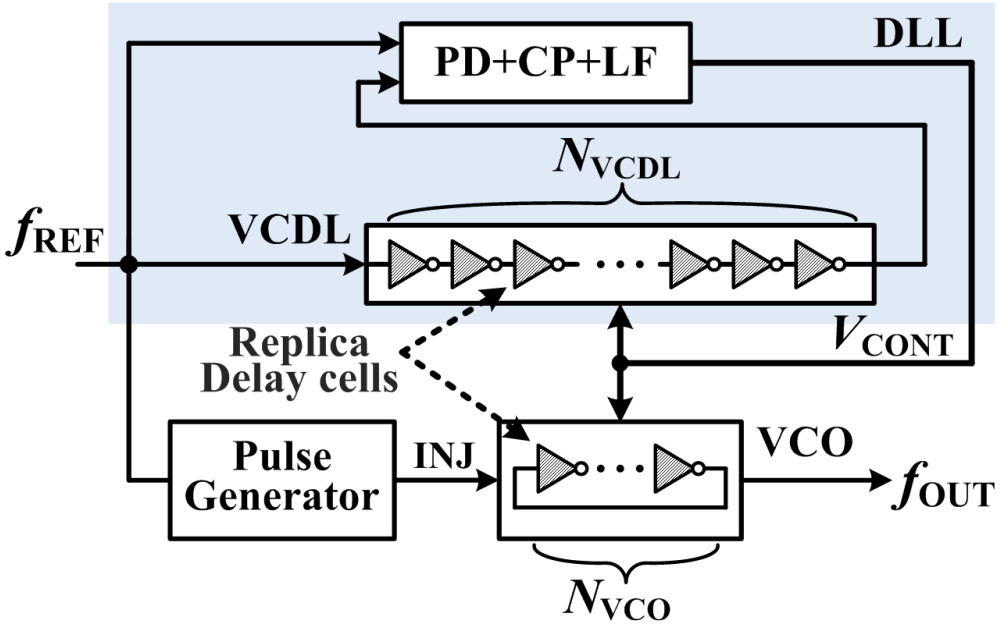
In this chapter, fractional-resolution ILCM using a DLL-based PVT calibrator is introduced. Compared to ILCMs, fractional-*N* PLLs can achieve very fine resolutions. However, they require a DSM and bulky passive components, which significantly increase the silicon area. Thus, if low-cost implementation of a clock generator is the primary goal, a fractional-resolution ILCM can be a preferred architecture as a clock generator. Although it cannot achieve a resolution as high as that of a fractional-*N* PLL, they have the benefit of a small area and low complexity.

Figure 17(a) shows the conceptual block diagram of the proposed DLL-based PVT-calibrator for fractional-resolution ILCMs. In the proposed architecture, the VCDL of the DLL and the ring-VCO consist of identical delay-cells, which share the same control voltage, V_{CONT}. When the DLL is locked, the total delay of the VCDL is fixed to the reference period, T_{REF}; thus, each delay cell of the VCDL can maintain accurate time information, independent of PVT variations. As shown in Figure 17(b), the unit delay of one delay-cell, T_{UNIT}, can be represented as T_{REF}/N_{VCDL}, where N_{VCDL} is the number of delay-cells of the VCDL. This time information, T_{UNIT}, is delivered to the delay cells of the VCO by the shared V_{CONT}, and it can define the free-running VCO frequency, f_{VCO}. When the number of the delay cells of the VCO is N_{VCO}, f_{VCO} can be represented as:

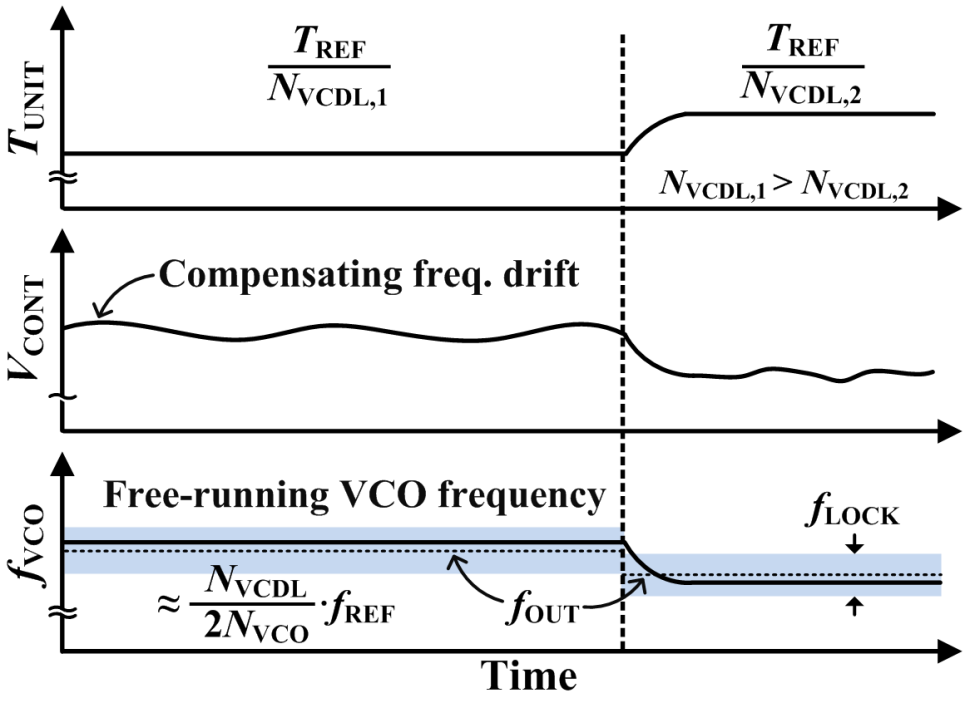
$$f_{VCO} \approx \frac{1}{2N_{VCO} \cdot T_{UNIT}} = \frac{N_{VCDL}}{2N_{VCO}} f_{REF} \tag{14}$$

As the DLL keeps adjusting V_{CONT} to maintain the constant delay of the VCDL, the VCO, which consists of the same delay cells, can also be continuously calibrated to maintain f_{VCO} close to the target frequency, f_{OUT}. In this work, we used the rotational injection technique in the injection-locked VCO, which will be discussed in detail in Section 4.1 [9]. Thus, an effective frequency-resolution of injection is a fractional f_{REF}. According to (14), the frequency resolution of the calibrator, i.e., $f_{REF}/(2N_{VCO})$, can be defined by properly selecting $2N_{VCO}$, and the target f_{VCO} can be switched by changing N_{VCDL}. Therefore, the proposed calibrator can easily move f_{VCO} close to any target frequencies with a fractional resolution without an additional complicated logic.

In the proposed PVT-calibrator, the VCO is not included in the loop; thus, the timing issue is no longer a concern. Even when the VCO is injection-locked, the delay cells in the VCDL can keep monitoring and detecting any instantaneous delay-disturbance caused by real-time variations of temperature or voltage. Therefore, the free-running VCO frequency (f_{VCO}) can be maintained very close to the target frequency (f_{OUT}), which prevents the degradation of jitter and the abrupt release of injection-locking. Since the proposed calibrator is based on a DLL, when the target frequency is switched, the frequency acquisition is faster than those of conventional architectures.



(a)

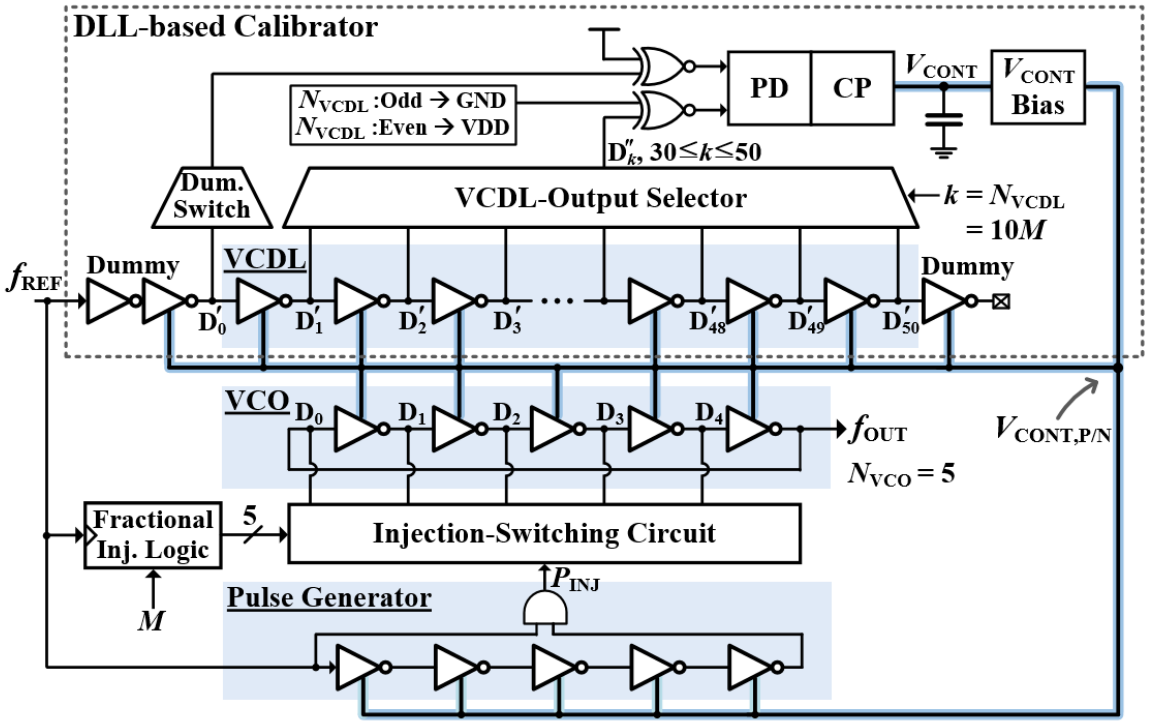


(b)

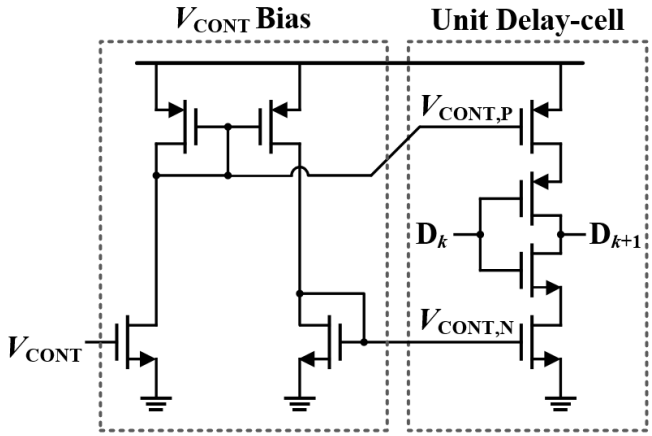
Figure 17. (a) Proposed DLL-based PVT-calibrator. (b) Operation of the DLL-based PVT-calibrator.

4.1. Implementation

Figure 18(a) shows the overall architecture of the proposed fractional-resolution ILCM, which consists of a ring-VCO, a DLL-based PVT-calibrator, a pulse generator, an injection-switching circuit, and a fractional-injection logic.



(a)



(b)

Figure 18. (a) Overall architecture of the proposed ILCM. (b) Schematics of an identical delay cell and a V_{CONT} bias circuit.

The delay cells in the VCO, the VCDL, and the pulse generator are identical, and they share the same control voltages, $V_{CONT,N}$ and $V_{CONT,P}$, generated by the V_{CONT}-bias circuit from V_{CONT}. The schematics of the unit delay-cell and the bias-circuit are shown in Figure 18(b). In this work, the number of delay cells of the VCO is fixed at five ($N_{VCO} = 5$); thus, f_{VCO} in (14) can be rewritten as:

$$f_{VCO} \approx \frac{N_{VCDL}}{10} f_{REF} = \left(Q + \frac{R}{10} \right) \cdot f_{REF} = M \cdot f_{REF}, \tag{15}$$

where Q and R are integers, and R is less than 10. According to (15), the multiplication factor, M, can be changed arbitrarily by selecting a different N_{VCDL}. In this design, N_{VCDL} can switch to any number between 30 and 50 by the VCDL-output selector; thus, any M between 3 and 5 with the step of 0.1 can be achieved. The range of M can be extended by using a larger N_{VCDL}. Since the DLL continuously monitors the real-time environmental variations and simultaneously adjusts T_{UNIT}, the deviation of f_{VCO} from f_{OUT} can be tightly controlled over time. Even if T_{UNIT} of the VCDL cannot be perfectly restored in the VCO due to practical issues, the inaccuracy of f_{VCO} is insignificant, compared to the lock range of the injection, f_{LOCK}.

The injection pulses generated by the pulse generator are injected into the VCO through the injection switching circuit. The switches of the injection switching circuit are controlled by fractional injection logic that consists of adders and D-flip-flops triggered by the reference clock. The fractional injection logic sends a five-bit control signal, corresponding to M, in every reference period. Since the pulse generator consists of the same delay-cells and shares V_{CONT}, the width of the injection pulses also can be regulated by the DLL. As noted, the lock range is maximized when the duty cycle of the injection-pulses is half the inverse of the multiplication factor [18]. Since the pulse generator includes five delay cells as the VCO, the duty cycle of the pulses is defined as N_{VCO}/N_{VCDL}, which is $1/(2M)$. Thus, the proposed ILCM can achieve the maximum lock range, independent of PVT variations and N_{VCDL}. To minimize the loading mismatch in the DLL design, dummy cells are connected before the first delay-cell of the VCDL and after the last (50th) delay-cell. The signal at D'_0 and that at another node, selected from D'_{30} to D'_{50} of the VCDL, are transferred to the PD through the VCDL-output selector, such that they are aligned with each other. The selection of the specific node is according to M and N_{VCDL} of (15). For example, if the target M is 3.6, N_{VCDL} equals 36, and the signal at D'_{36} is delivered. Each input of the PD is preceded by one XNOR gate. This is because for even N_{VCDL}, the rising edges of the signal from the output selector are aligned with the reference, whereas for odd N_{VCDL} the falling edges of the signal from the output selector are aligned with the reference. A dummy switch is located in the path between D'_0 and the XNOR gate to remove the delay mismatch caused by the VCDL-output selector. The structures of the dummy switch and the VCDL output selector are basically

the same, but only one of the inputs is used in the former as shown in Figure 19. Since both outputs of the dummy switch and the VCDL output selector are loaded by one on-switch, 49 off-switches, and input transistors of a XNOR gate, capacitive loadings were balanced.

Figure 20 shows the details of the VCDL-output selector and the injection-switching circuit. In order to minimize mismatches, the capacitive loadings of the delay cells of the VCO and the VCDL were matched precisely at the schematic level using transmission-gate switches.

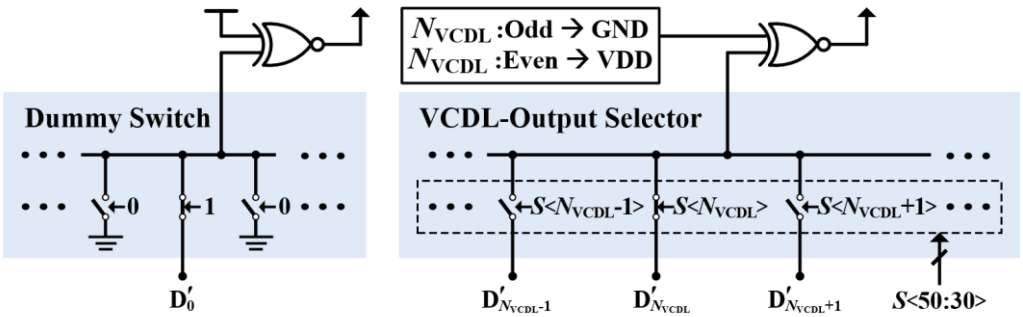


Figure 19. Schematics of the dummy switch and the VCDL-output selector

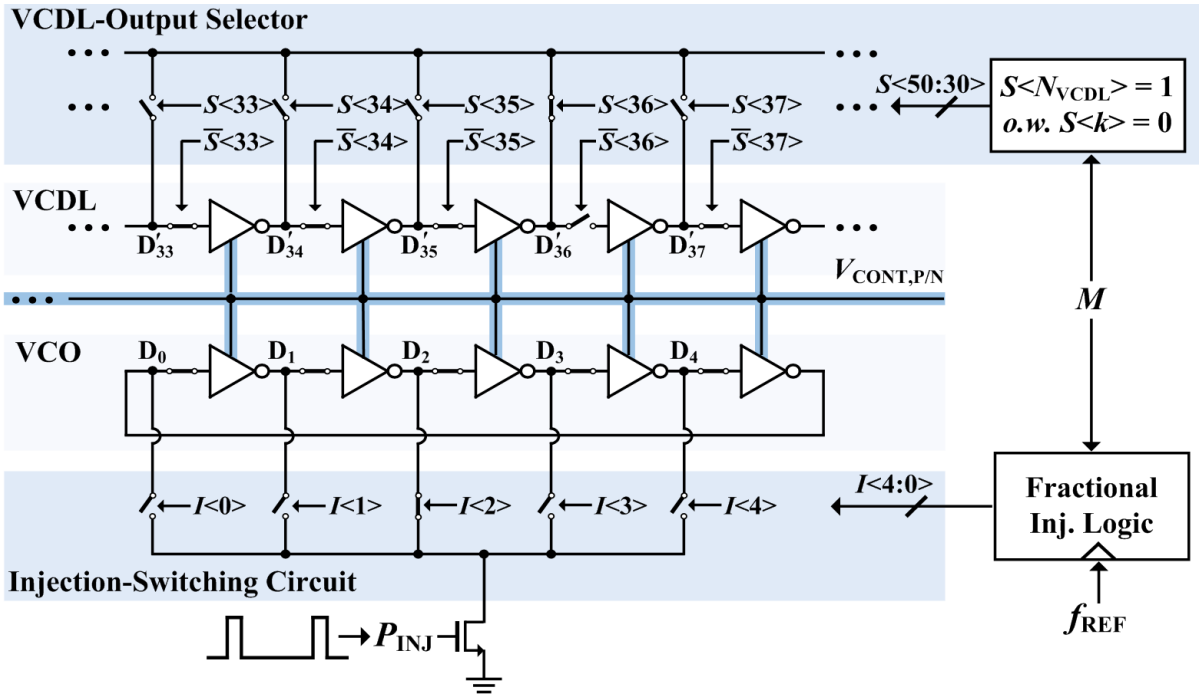


Figure 20. Implementation of the switches in the VCDL-output selector and the injection-switching circuit to reduce loading mismatches (N_{VCDL} = 36).

In the VCDL, there is a parallel switch at the output of each delay cell to change N_{VCDL}. Only the switch of the N_{VCDL}^{th} delay cell is turned on to send its output to the PD. To match the loading of other delay cells with that of the N_{VCDL}^{th} delay cell of the VCDL, one additional series switch was inserted between the delay cells. All series switches except the one that follows the N_{VCDL}^{th} cell are turned on; thus, each cell of the VCO, the VCDL, and the pulse generator includes one on-switch and one off-switch at the output. In the VCO, parallel switches are used for injection, and one of them is turned on briefly during its turn of injection.

To realize the effect of injection with a frequency of a non-integer multiple of f_{REF}, the injection point of the VCO, from D_0 to D_4, is rotated periodically by the injection switching circuit, based on the algorithm of the fractional injection logic. Figure 21 shows a phase diagram that represents the sequential rotation of the injection point of the VCO in two cases, i.e., when R of (15) is either 2 or 3. Since the VCO consists of five single-ended delay cells, it generates five rising edges during one period, T_{REF}, which is sequentially presented as D_0, D_2, D_4, D_1, and D_3 in the phase diagram of Figure 21. When R is an even number, the injection point of the VCO is rotated by $2\pi \cdot M$ in the clockwise direction during T_{REF}, which results in the effective phase shift of $2\pi \cdot (R/10)$. For example, when M equals 3.2 (Q = 3, R = 2), the injection point is shifted by two steps in every period, i.e., $D_0 \rightarrow D_2 \rightarrow D_4 \rightarrow D_1 \rightarrow D_3$. When R is an odd number, the injection point is also rotated effectively by $2\pi \cdot (R/10)$ during T_{REF}, but the pulse is injected in every second period in this case. This is because the injection pulse should be aligned to either the rising or falling edge, since the VCO is a single-ended structure. When M is 3.3 (Q = 3, R = 3), the injection point is shifted by three steps in every period, and the injection is done in every second period. Therefore, the sequence of the injecting point becomes $D_0 \rightarrow X \rightarrow D_1 \rightarrow X \rightarrow D_2 \rightarrow X \rightarrow D_3 \rightarrow X \rightarrow D_4 \rightarrow X$, where X indicates no injection. The sequences of the injection point for all Rs were provided in Table 1. The effective frequency-resolution of the fractional injection of this injection logic is $f_{REF}/(2N_{VCO})$. Since the proposed calibrator can move the VCO frequency to the vicinity of any multiples of $f_{REF}/(2N_{VCO})$ according to (15), it can properly calibrate the VCO frequency in any cases of the factional injection logic above.

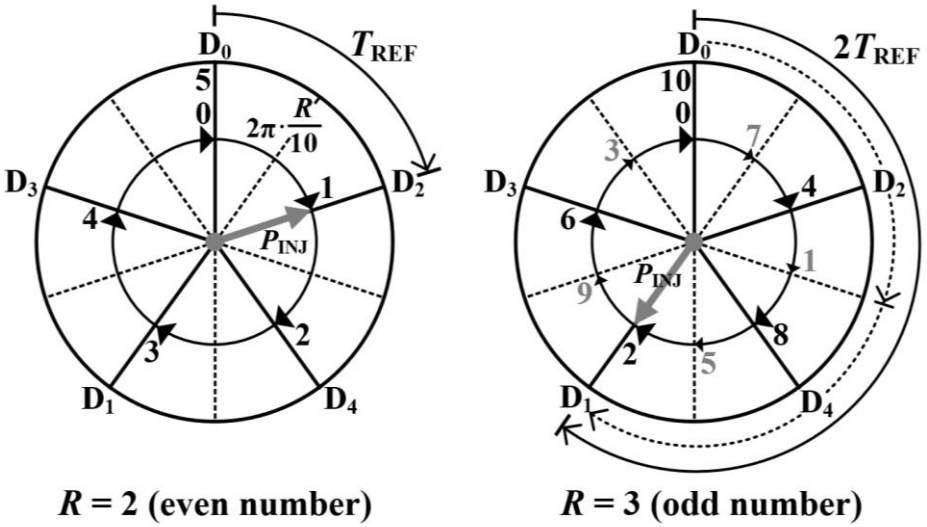


Figure 21. Rotations of the injection point when R equals 2 and 3 by the fractional injection logic.

Table 1. Sequences of the injection point.

R	Injection sequence
0	$D_0 \rightarrow \cdots$
1	$D_0 \rightarrow X \rightarrow D_2 \rightarrow X \rightarrow D_4 \rightarrow X \rightarrow D_1 \rightarrow X \rightarrow D_3 \rightarrow X \rightarrow \cdots$
2	$D_0 \rightarrow D_2 \rightarrow D_4 \rightarrow D_1 \rightarrow D_3 \rightarrow \cdots$
3	$D_0 \rightarrow X \rightarrow D_1 \rightarrow X \rightarrow D_2 \rightarrow X \rightarrow D_3 \rightarrow X \rightarrow D_4 \rightarrow X \rightarrow \cdots$
4	$D_0 \rightarrow D_4 \rightarrow D_3 \rightarrow D_2 \rightarrow D_1 \rightarrow \cdots$
5	$D_0 \rightarrow X \rightarrow \cdots$
6	$D_0 \rightarrow D_1 \rightarrow D_2 \rightarrow D_3 \rightarrow D_4 \rightarrow \cdots$
7	$D_0 \rightarrow X \rightarrow D_4 \rightarrow X \rightarrow D_3 \rightarrow X \rightarrow D_2 \rightarrow X \rightarrow D_1 \rightarrow X \rightarrow \cdots$
8	$D_0 \rightarrow D_3 \rightarrow D_1 \rightarrow D_4 \rightarrow D_2 \rightarrow \cdots$
9	$D_0 \rightarrow X \rightarrow D_3 \rightarrow X \rightarrow D_1 \rightarrow X \rightarrow D_4 \rightarrow X \rightarrow D_2 \rightarrow X \rightarrow \cdots$

***** X indicates no injection.

Figure 22 shows the block diagram of the fractional injection logic, which consists of an accumulator with a reset logic, a divide-by-2 frequency divider, and other logics. The output of the fractional injection logic, *I*, controls the switches connected to the VCO, where the injection point is D_I. *R* becomes an input of the accumulator. The reset logic of the accumulator ensures that the output is an integer among 0, 1, 2, 3, and 4. When *I* becomes 5, injection is skipped, since none of the switches are turn on.

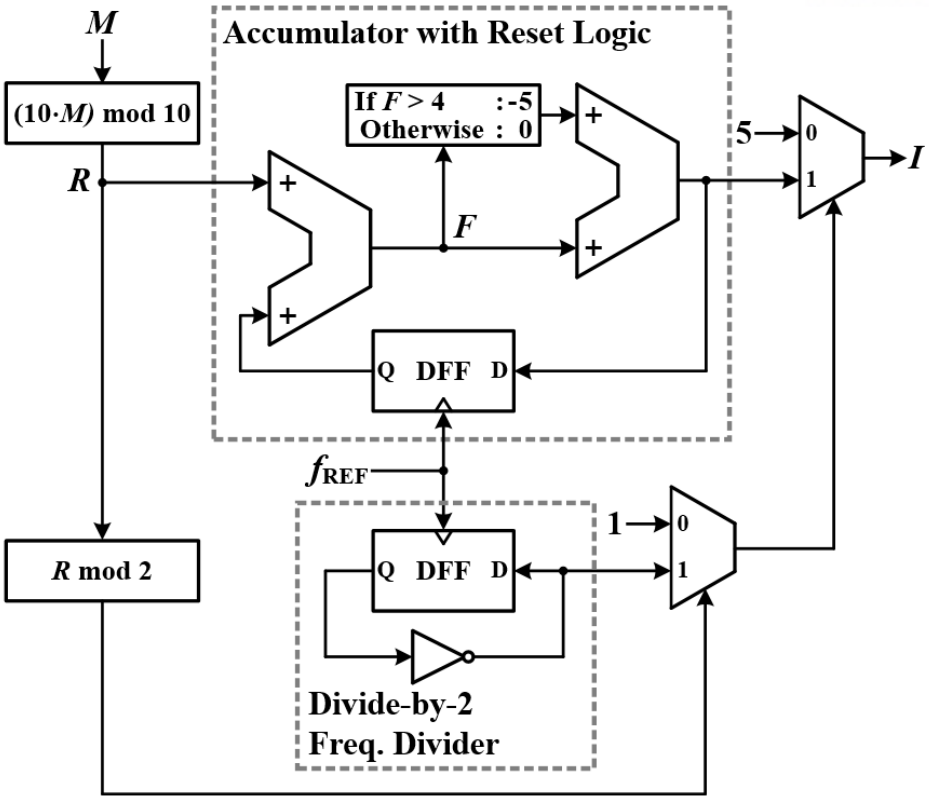


Figure 22. Block diagram of the fractional injection logic.

4.2. Analysis of phase noise and spurs

4.2.1. Noise modeling for the proposed ILCM

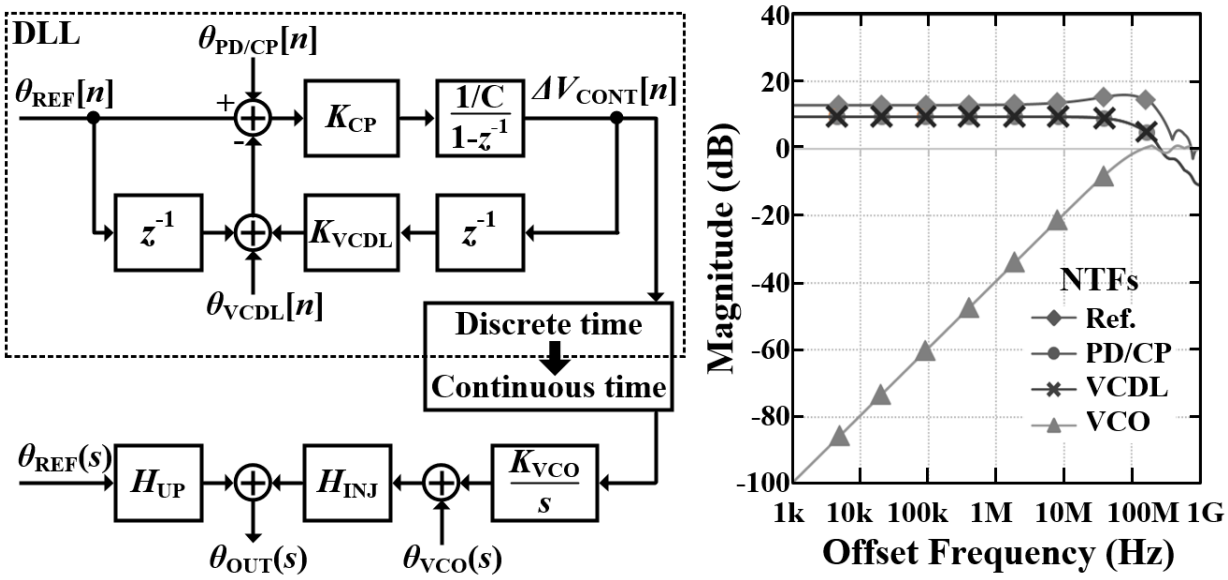
Figure 23(a) shows the noise model of the proposed ILCM. Each building block of the DLL was modeled in the discrete time domain. The units of the gains of the VCDL, K_{VCDL}, and the PD and the charge pump (CP), $K_{PD/CP}$, are [rad/V] and [A/rad], respectively. θ_{REF} and θ_{VCDL} are the output-referred phase errors of the reference clock and the VCDL, respectively, and $\theta_{PD/CP}$ is the input-referred phase error of the PD/CP. Transfer functions from the reference clock, $H_{REF}(z)$, the PD/CP, $H_{PD/CP}(z)$, and the VCDL, $H_{VCDL}(z)$, to the control voltage can be represented as

$$H_{REF}(z) = \frac{\Delta V_C(z)}{\theta_{REF}} = \frac{K_{CP}}{C} \frac{1-z^{-1}}{1-(1-K_{CP}K_{VCDL}/C)z^{-1}}, \quad (16)$$

$$H_{PD/CP}(z) = \frac{\Delta V_C(z)}{\theta_{PD/CP}} = \frac{K_{CP}}{C} \frac{1}{1-(1-K_{CP}K_{VCDL}/C)z^{-1}}, \quad (17)$$

$$\text{and} \quad H_{VCDL}(z) = \frac{\Delta V_C(z)}{\theta_{VCDL}} = -\frac{K_{CP}}{C} \frac{1}{1-(1-K_{CP}K_{VCDL}/C)z^{-1}}, \quad (18)$$

respectively, where C is the capacitance of the loop filter [21].



(a) (b)

Figure 23. (a) Noise model of the proposed ILCM using a DLL-based PVT calibrator. (b) NTFs of building blocks based on (21)–(24).

Then, each transfer function is converted to the equivalent function in the continuous time domain, and multiplied by the transfer function of the VCO, K_{VCO}/s. The phase-realignment by the reference clock can be modeled by following two transfer functions [2], [3]:

$$H_{INJ}(j\omega) = 1 - \frac{\beta \cdot e^{-j\omega T_{REF}/2}}{1+(\beta-1)e^{-j\omega T_{REF}}} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}, \tag{19}$$

$$\text{and} \quad H_{UP}(j\omega) = \frac{N \cdot \beta \cdot e^{-j\omega T_{REF}/2}}{1+(\beta-1)e^{-j\omega T_{REF}}} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}, \tag{20}$$

where β is the phase realignment factor. From (16) – (20), the noise transfer functions (NTFs) to the output of the injection-locked VCO from the reference clock, $T_{REF}(j\omega)$, the PD/CP, $T_{PD/CP}(j\omega)$, the VCDL, $T_{VCDL}(j\omega)$, and the VCO, $T_{VCO}(j\omega)$, can be expressed as:

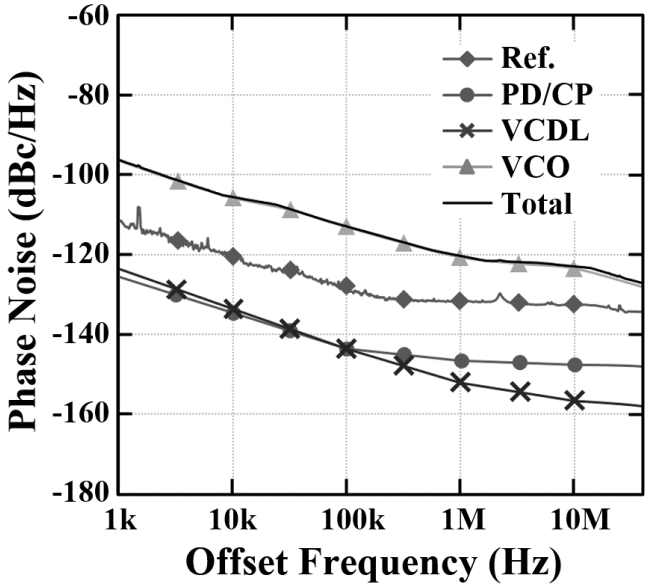
$$T_{REF}(j\omega) = \frac{\theta_{OUT}}{\theta_{REF}} = H_{UP}(j\omega) + H_{REF}(j\omega)\frac{K_{VCO}}{j\omega}H_{INJ}(j\omega), \tag{21}$$

$$T_{PD/CP}(j\omega) = \frac{\theta_{OUT}}{\theta_{PD/CP}} = H_{PD/CP}(j\omega)\frac{K_{VCO}}{j\omega}H_{INJ}(j\omega), \tag{22}$$

$$T_{\mathrm{VCDL}}(j\omega)=\frac{\theta_{\mathrm{OUT}}}{\theta_{\mathrm{VCDL}}}=H_{\mathrm{VCDL}}(j\omega)\frac{K_{\mathrm{VCO}}}{j\omega}H_{\mathrm{INJ}}(j\omega), \tag{23}$$

$$\text{and}\quad T_{\mathrm{VCO}}(j\omega)=\frac{\theta_{\mathrm{OUT}}}{\theta_{\mathrm{VCO}}}=H_{\mathrm{INJ}}(j\omega), \tag{24}$$

respectively. The NTFs of the building blocks, (21) – (24), were plotted in Figure 23(b). For NTFs, $K_{\mathrm{PD/CP}}$, K_{VCO}, K_{VCDL}, C, and N were 31.8 μA/rad, 1.8 GHz/V, 6.5 rad/V, 9.5 pF, and 4.4, respectively. The output frequency was 1.76 GHz, and β was 0.85. As shown in the Figure 23(b), the NTF of the VCO is high-pass-shaped due to $H_{\mathrm{INJ}}(j\omega)$. Although the NTF of the reference clock consists of two terms according to (21), it is low-pass-shaped since $H_{\mathrm{UP}}(j\omega)$ is dominant. The NTFs of the PD/CP and the VCDL are also low-pass-shaped, since a high-pass filtering effect of $H_{\mathrm{INJ}}(j\omega)$ is cancelled by the origin pole of the transfer function of the VCO. The NTFs can be used to estimate the total phase noise and evaluate the noise contribution of each building block. The phase noise curves in Figure 24 were plotted using MATLAB. The noise data of the reference clock was based on measurements, and those of other circuits were from post-layout simulations. As shown in the figure, the most dominant noise source is the ring-VCO, which contributed approximately 91% of the total phase noise. This is because the low-power ring-VCO in this work had a poor noise performance and also its flicker noise was not sufficiently suppressed by the first-order high-pass filter of $T_{\mathrm{VCO}}(j\omega)$. The noise contribution of the DLL was less than 0.5%, which confirmed the proposed DLL-based calibrator would not degrade the phase noise performance of the clock multiplier.



	IPN (dBc) 1 k – 40 MHz	Contribution (%)
VCO	-44.805	91.214
Ref.	-55.196	8.336
PD/CP	-68.534	0.386
VCDL	-76.372	0.064

Figure 24. Phase noises and noise contributions of building blocks based on the noise model.

4.2.2. Analysis of phase noise degradation caused by the mismatch between delay cells

The fundamental assumption of the proposed architecture is that each delay cell of the VCDL and the VCO has exactly the same delay. Based on this assumption, the VCO can generate a precise output frequency that is very close to the target frequency. Therefore, it is important to match the capacitive loadings carefully in the schematic and place all delay cells close together in the layout. However, despite these efforts, inevitable mismatches could occur between the delay cells of the VCDL and the VCO. If the mismatches become severe due to local process variations, the free-running VCO frequency deviates from the target frequency, which causes the significant degradation of jitter or phase noise. Figure 25 shows the possible frequency deviation of the VCO frequency from the target frequency of 1.6 GHz, Δf_{VCO}, due to mismatches between the delay cells of the VCO and the VCDL from the Monte Carlo simulation. As shown in Figure 25, the worst Δf_{VCO} is 18 MHz, which corresponds to 1.1% of 1.6 GHz. Another possible cause of the frequency deviation is the static offset of the DLL. It was simulated as 10 ps in this work, corresponding to 0.4%. As noted, the sensitivity of the noise performance of an ILCM to Δf_{VCO} varies according to β. Figure 26 shows the degradation of spot noise according to β from 0.65 to 0.99, when Δf_{VCO} increased to 1.5%. Actually, β is a function of Δf_{VCO}. Therefore, β in Figure 26 represents the value of β when Δf_{VCO} is zero. In the simulation, β was scaled by changing the injection strength. As shown in Figure 26, phase noise degradations at all three offsets, 100 kHz, 1 MHz, and 10 MHz, were less than 1.0 dB when β was 0.8. This implies that if β is designed as larger than 0.8, the degradation of phase noise can be restricted to less than 1.0 dB even in the worst case.

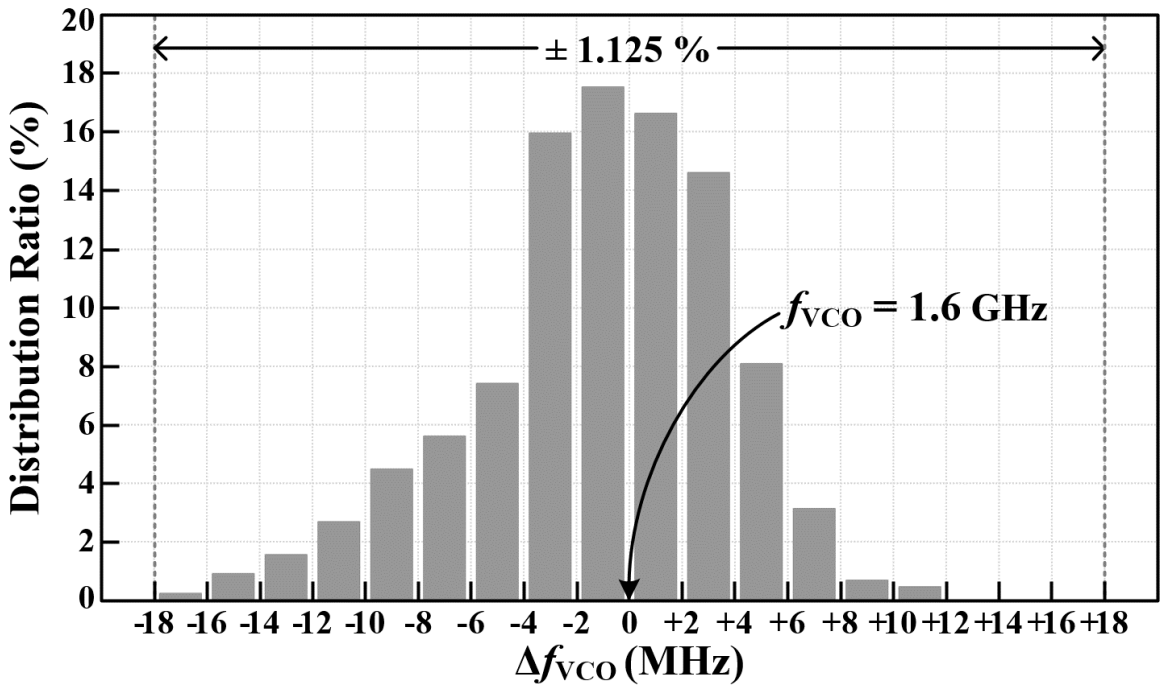


Figure 25. Variation of Δf_{VCO} due to mismatches between delay cells in the VCDL and the VCO from the Monte-Carlo simulation.

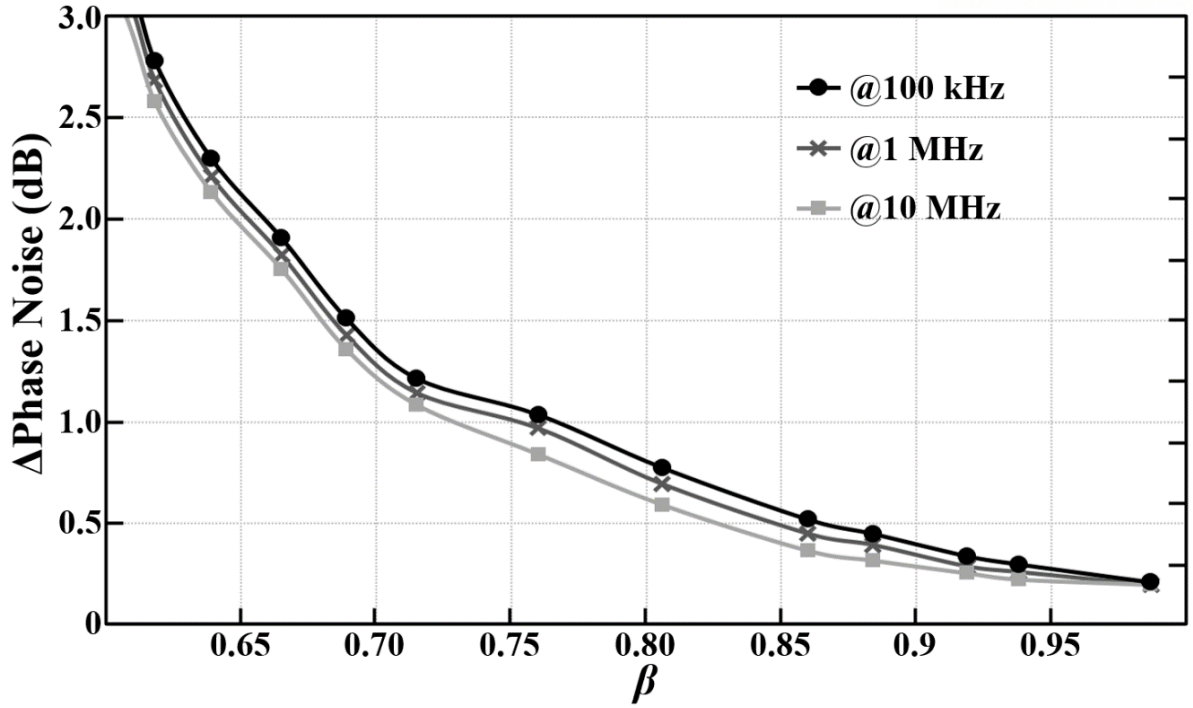


Figure 26. Phase-noise degradation according to $\beta(\Delta f_{VCO} = 0)$, when Δf_{VCO} increased to 1.5%.

4.2.3. Levels of spurious tones

In the proposed ILCM, if the DLL has large CP up/down current mismatch and current-leakage through the loop filter, the periodic disturbance of V_{CONT} will cause the reference spur at the offset of f_{REF} from the center frequency. Considering the CP current-mismatch as the major cause of the reference spur, the level of the spur can be represented as [22]:

$$SP_{DLL} = 20\log\left(\frac{i_{CP\_Fref} \cdot K_{VCO}}{4\pi \cdot C \cdot f_{REF}^{2}}\right), \tag{25}$$

where i_{CP_Fref} is the amplitude of the fundamental component of the current ripple at the CP output. C and K_{VCO} were designed as 9.5 pF and 1.8 GHz/V, respectively, and i_{CP_Fref} was less than 2 μA from post-layout simulations. Thus, according to (25), SP_{DLL} can be expected to be less than –70 dBc. The difference between the free-running VCO frequency and the target frequency also causes spurs. The level of this spur can be represented as [13]:

$$SP_{\Delta Fvco} = 20\log\left(\frac{M \cdot \Delta}{2T_{REF}}\right), \tag{26}$$

where Δ is the time-error of the VCO's signal, which is supposed to be corrected by the injection. The spur level according to the frequency deviation when M is 4 is plotted in Figure 27. According to the results of the Monte-Carlo simulation in Figure 25, $SP_{\Delta FVCO}$ can be estimated to increase up to –34 dB in the worst case.

When the multiplication factor, M, is an integer (R = 0), the proposed clock multiplier operates just as a conventional sub-harmonic architecture does, and thus, spurs are present at the offset of f_{REF}. Also, when R is 5, the effective frequency of the injection clock becomes $f_{REF}/2$, and the injection point is fixed as in the conventional sub-harmonic ILCMs. Therefore, spurs are presented at the offset of $f_{REF}/2$ in this case. However, when R is not 0 or 5, the injection-point of the VCO rotates periodically. Thus, the effective period of the injection is extended with respect to one node of the VCO. As a result, the spurs occur closer to the output frequency; the offset frequency of the spurs becomes $f_{REF}/5$ or $f_{REF}/10$ for even and odd values of R, respectively.

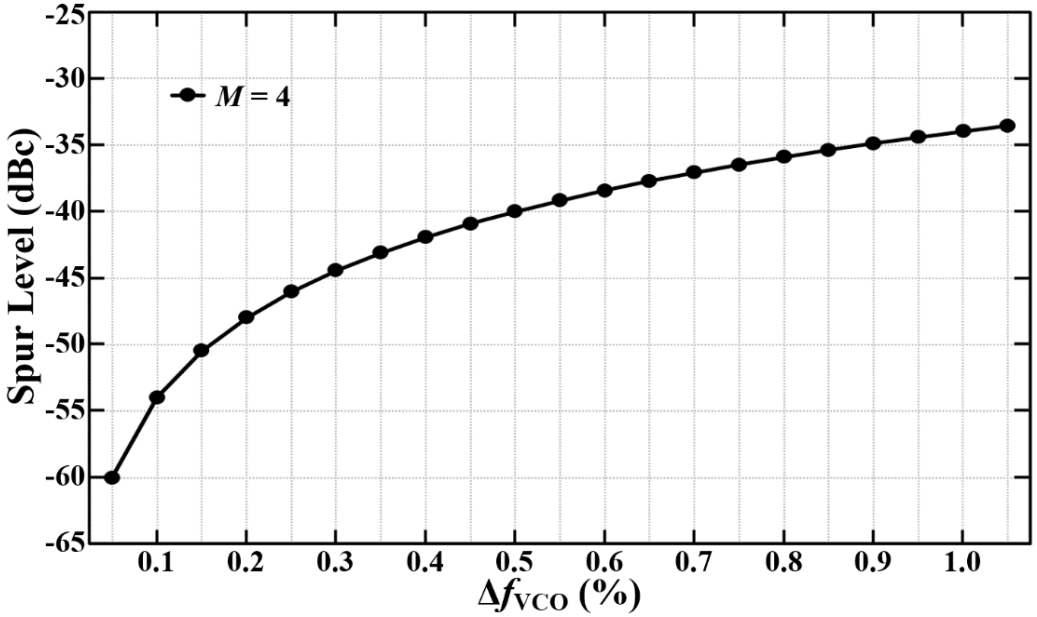


Figure 27. Spur level according to (26) when M = 4 (f_{OUT} = 1.6 GHz).

V. Experimental results

5.1. Dual-loop ILCM using a two-phase PVT-calibrator

The dual-loop ILCM was designed with the prototype PLL and fabricated in a 65-nm CMOS process as shown in Figure 28. The active area of the ILCM was 0.062 mm^2, and the PLL, including the test-pads, occupied 1.46 mm^2. The total power consumption of the ILCM was 1.9 mW, when the output frequency of the ILCM was 96 MHz.

Figure 29(a) and (b) show output spectrums, which was measured using a spectrum analyser, Agilent N9030A, when the output frequencies of the ILCM were 57.6 and 96 MHz, respectively. Figure 30(a) and (b) show phase noise measured using a signal source analyser, Agilent E5052B, when the output frequencies of the ILCM were 57.6 MHz and 96 MHz. In Figure 30(a), without injection, the spot noise of the free-running VCO was −76.2, −99.5, and −120.0 dBc/Hz at the 10 k, 100 k, and 1 MHz offsets, respectively. However, when injection locked, it showed a dramatic improvement of phase noise; thus, spot noise at the same offsets were reduced to −131.4, −133.9, and −137.2 dBc/Hz, respectively. Similarly, Figure 30(b) also shows the dramatic improvements of phase noise. When the integration range is from 1 kHz to 10 MHz, the RMS-jitter was 1.69 ps.

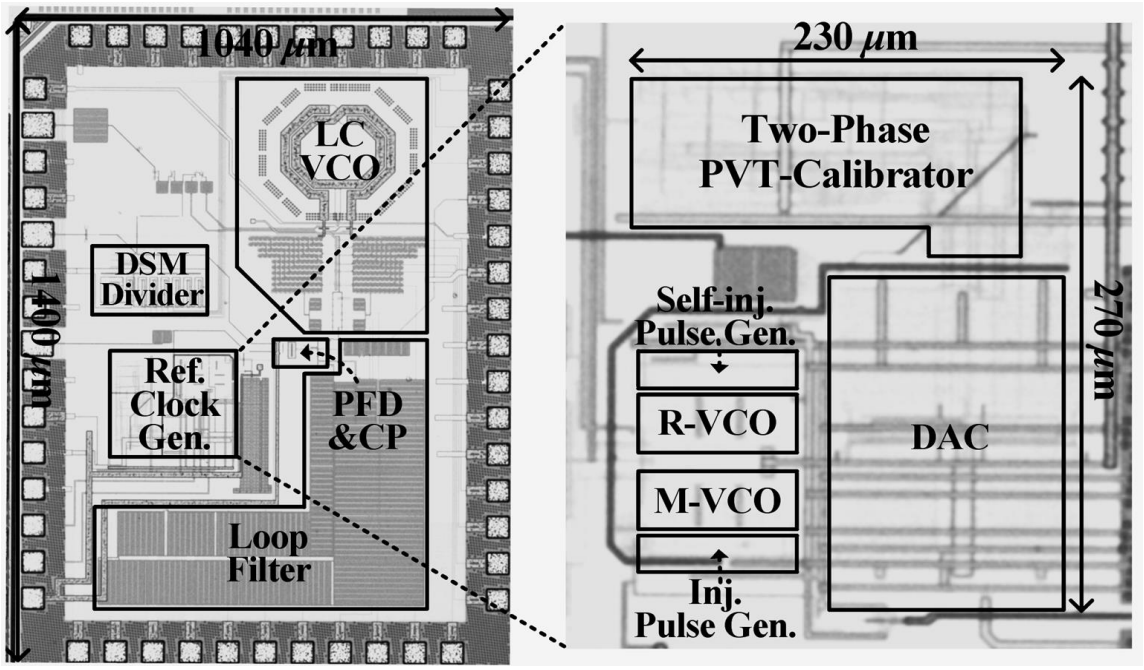
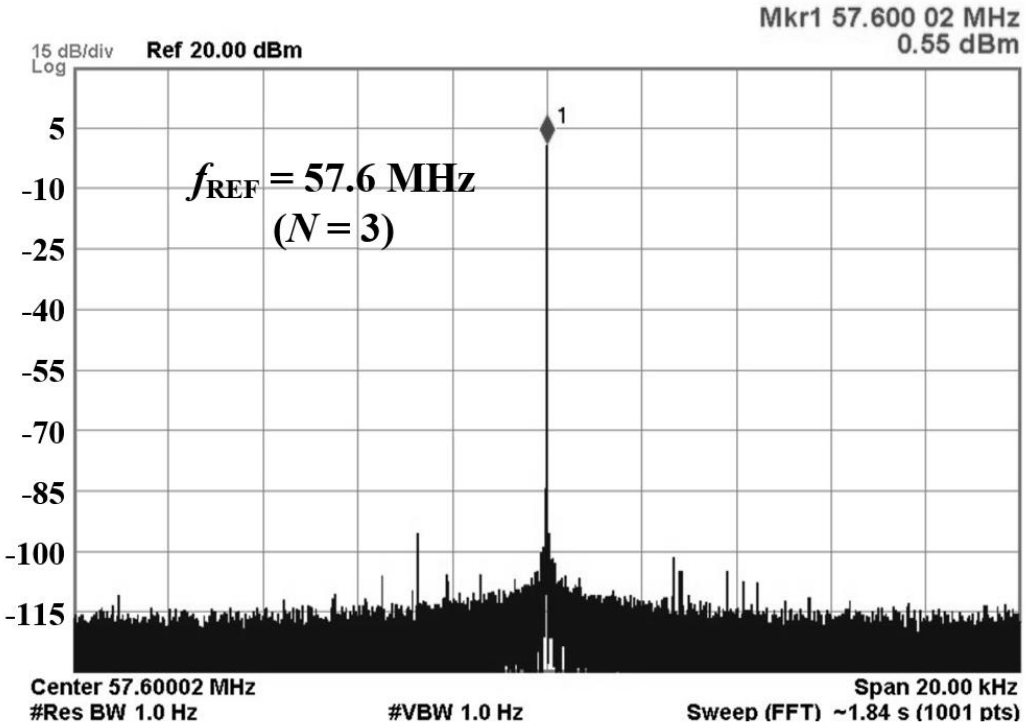
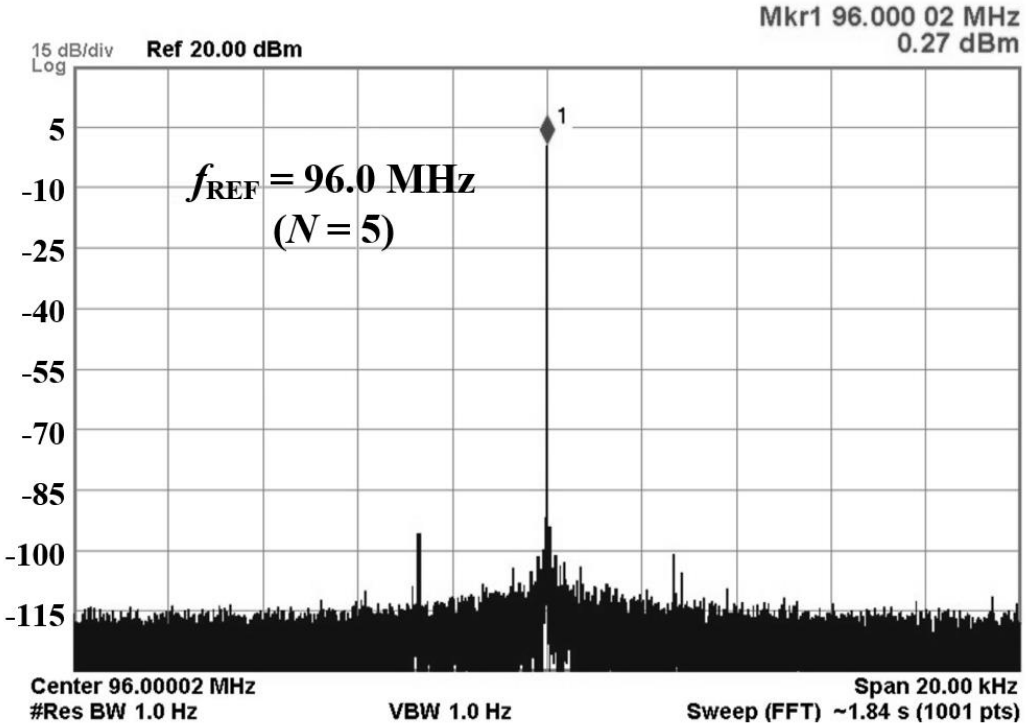


Figure 28. Microphotograph of the prototype PLL with the proposed ILCM.

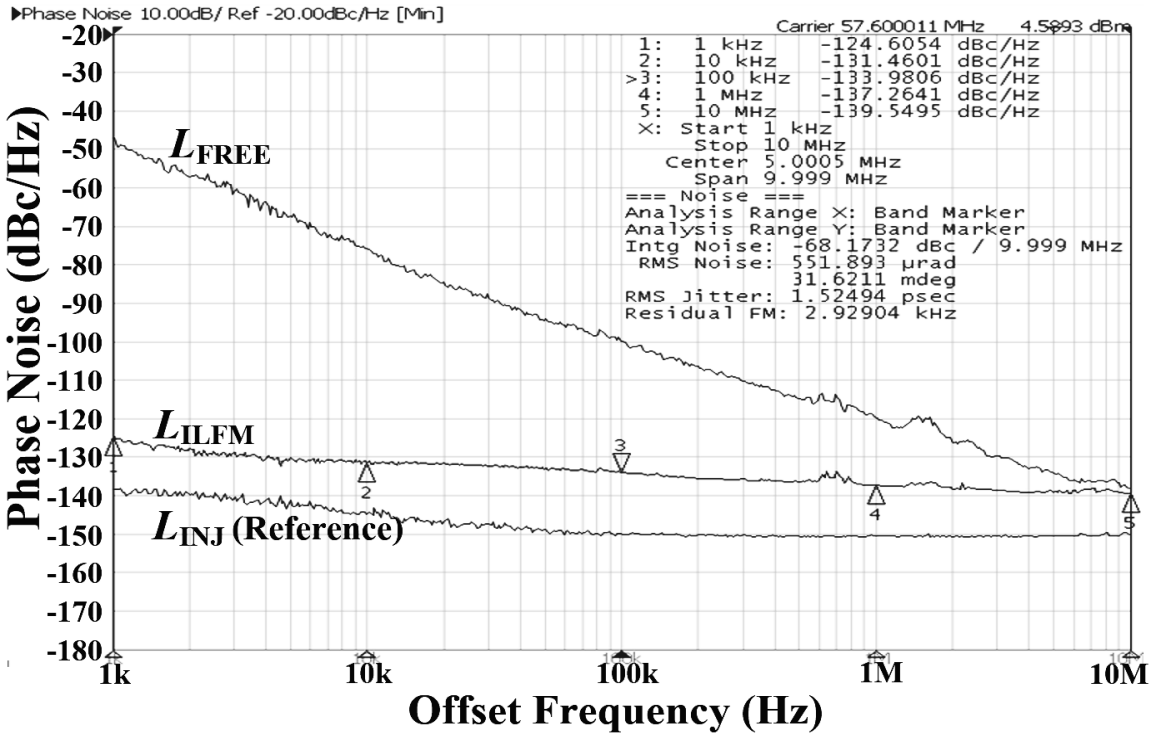


(a)

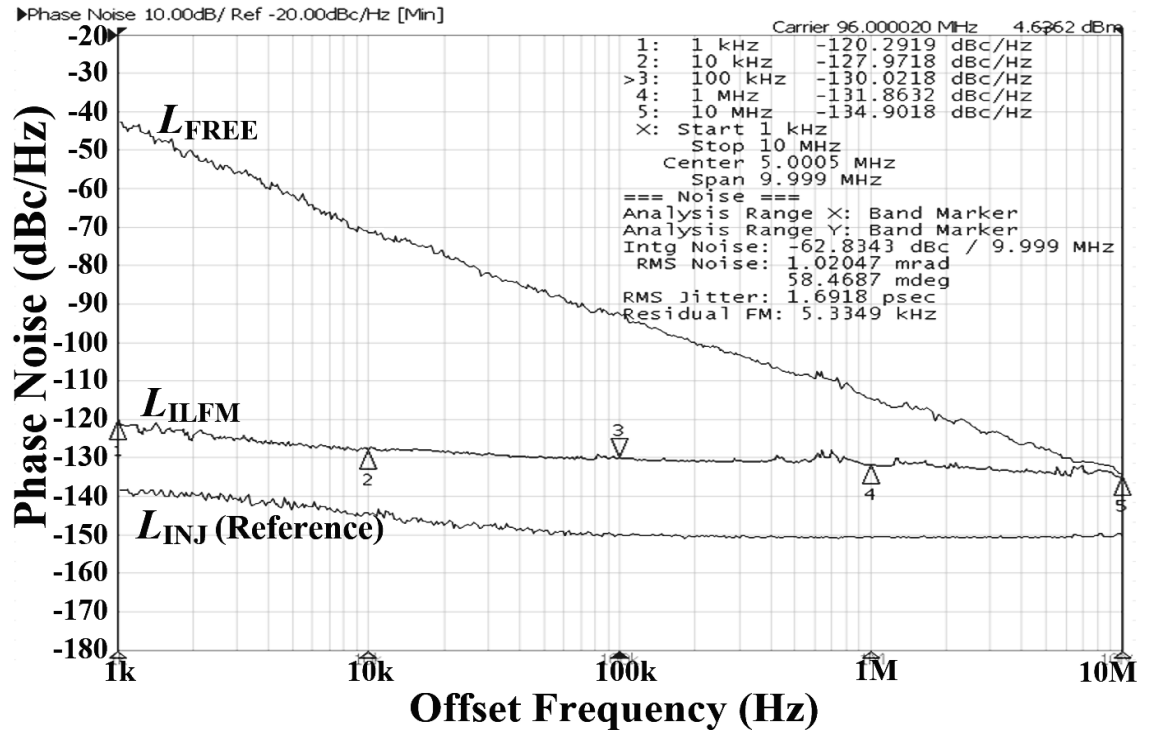


(b)

Figure 29. Measured spectrum of the proposed ILCM when f_{REF} equals 57.6 MHz (b) 96 MHz



(a)



(b)

Figure 30. Measured phase noise of the proposed ILCM when f_{REF} equals (a) 57.6 MHz (b) 96 MHz.

Figure 31 compares the variations of the measured phase noise according to changes in the temperature, either when the calibrator was turned off or on. When the temperature changed from 30 to 80 ℃, the free-running frequency of the VCO was varied from 57.6 to 61 MHz. In this experiment, the PVT-calibrator was turned off after the first-phase calibration in the first measurement, and kept on in the second measurement while the temperature was swept. When the calibrator was turned-off, phase noise was sharply degraded as the temperature increased, and the injection-lock was released above 70℃. When the calibrator was kept on, the phase noise degradation was restricted to less than 0.5 dB.

Figure 32 shows the measured phase noise of the output signal of the PLL with a 4.4 GHz frequency, according to different f_{REF}. The bandwidth of the PLL was 100 kHz. When f_{REF} was 19.2 MHz, the phase noise curve has a massive noise hump from the DSM around 100 k – 20 MHz offsets. When f_{REF} was 57.6 MHz, the noise hump was reduced, and it was totally disappeared when f_{REF} was increased to 96 MHz.

Figure 33 shows the measured output spectrum of the PLL when f_{REF} was 96 MHz. The level of the spur at the 19.2-MHz offset was –39 dBc at the output of the ILCM, but it was less than –70 dBc at the output of the PLL because of low-pass filtering of the PLL. Table 2 compares the performance of the proposed ILCM with state-of-the-art architectures.

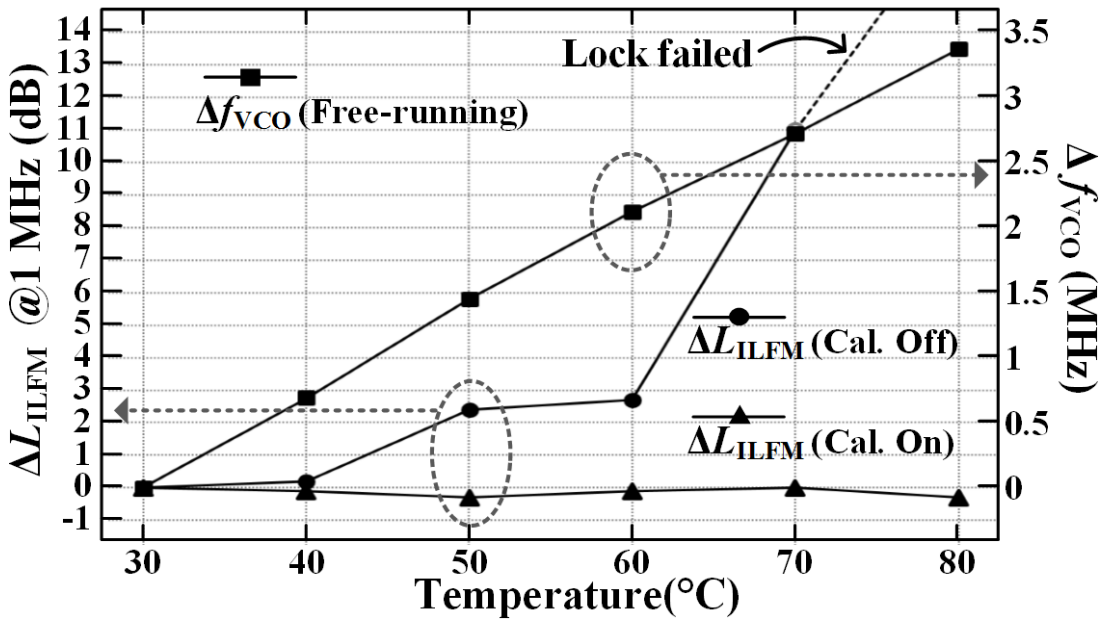


Figure 31. Variation of phase noise of the proposed ILCM at 1 MHz offset over temperature.

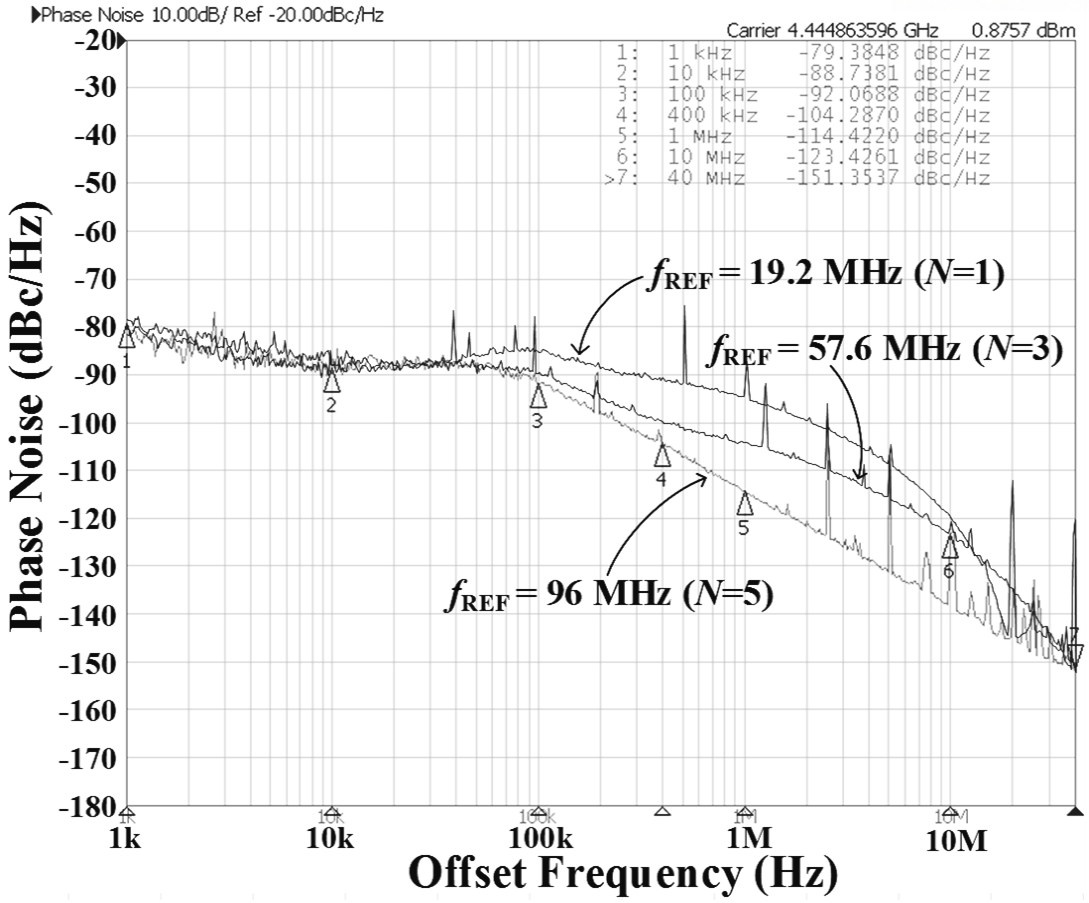


Figure 32. Measured phase noise of the prototype PLL when f_{REF} equals 4.4 GHz.

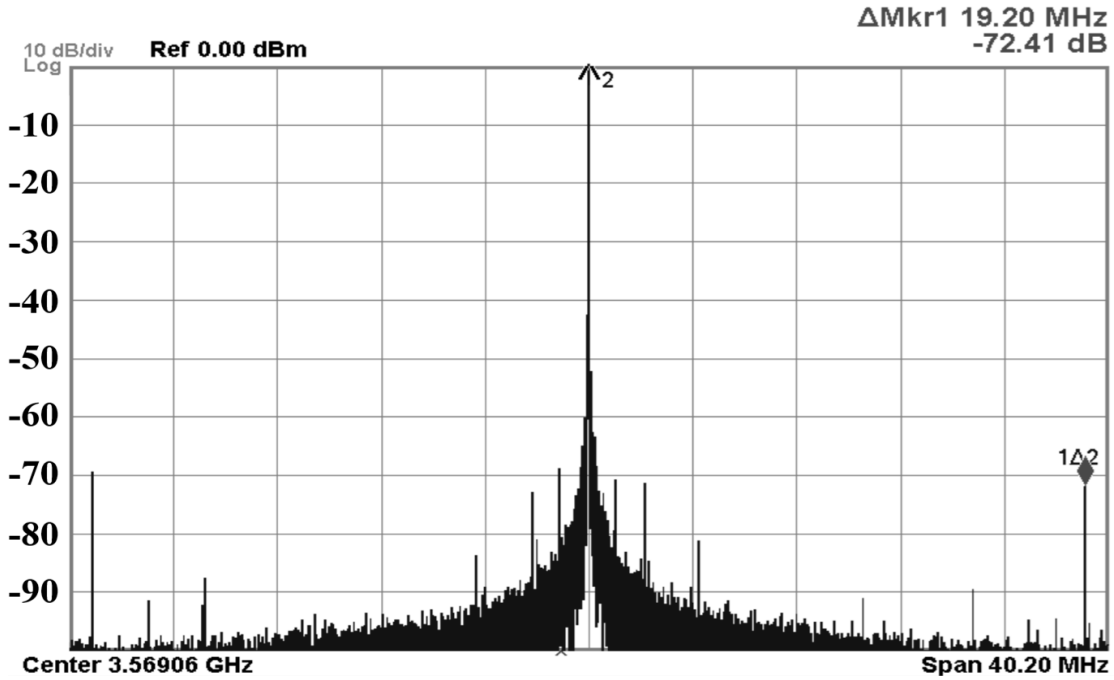


Figure 33. Measured spectrum of the prototype PLL when f_{REF} equals 96 MHz.

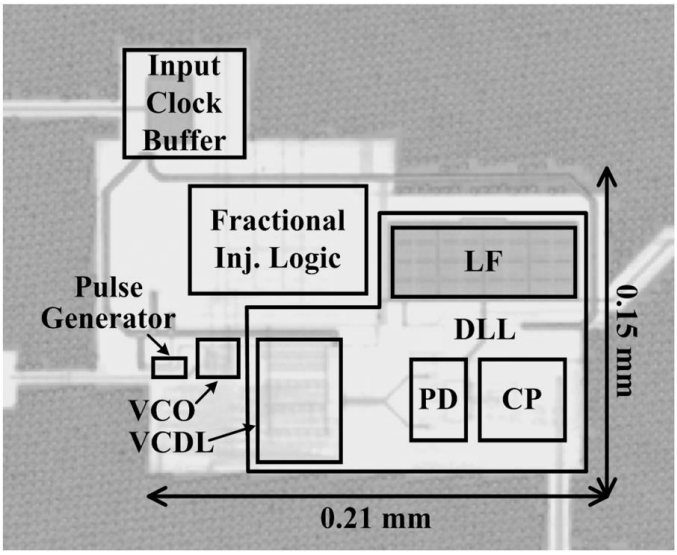
Table 2. Performance comparison with the state-of-the-art ILCMs

	[13]	[16]	[9]	[15]	This work	
Process (CMOS)	65 nm	55 nm	65 nm	65 nm	65 nm	
Topology	IL + CAL	PLL + IL	PLL + IL	IL + CAL	IL + CAL	
Ref. Clk Freq. (Hz)	300 M	27 M	32 M	150 M	19.2 M	
Output Freq. (f_O) (Hz)	1200 M	216 M	580 M	900 M	57.6 M	96.0 M
PN (dBc/Hz) @ f_{OFF}	–100 @100k	–123.5 @100k	–104 @100k	–104 @100k	–134.0 @100k	–130.0 @100k
Ref. Clk PN + 20log(N) (dBc/Hz)	NA	–128.3 @100k	NA	–138 @100k	–140.1 @100k	–135.7 @100k
Integ. Jitter (σ_t) (s)	0.7p (10k – 40 M)	2.4p (1k – 40 M)	2.45p (100 – 40 M)	1.7 p (10k – 40M)	1.52 p (1k – 10M)	1.69 p (1k – 10M)
P_{DC} (mW)	0.97	6.9	10.5	0.78	1.6	1.9
FOM_jitter (dB)	–243.2	–224.0	–222.0	–236.4	–234.3	–232.7
PN Degradation over Temp.	<5p (p-p jitter) <0.5p (rms jitter)	NA	NA	NA	< 0.5 dB	
Active area (mm^2)	0.022	0.03	0.158	0.0066	0.062	
Freq. Acq. Time (s)	NA	NA	NA	NA	< 10 μ	

***** FoM: $10 \cdot \log10(\sigma_t^2 \cdot P_{DC})$ dB

5.2. Fractional-resolution ILCM using a DLL-based PVT-calibrator

The fractional-resolution ILCM using a DLL-based PVT-calibrator was fabricated in a 65-nm CMOS process, as shown in Figure 34. It occupied an active area of 0.032 mm^2 and consumed 3.6 mW from the 1.2-V supply. The proposed ILCM achieved a multiplication factor from 3 to 5 with a 0.1 step, thereby generating output frequency ranging from 1.2 to 2.0 GHz with a resolution of 40 MHz when a reference clock with a frequency of 400 MHz is used.



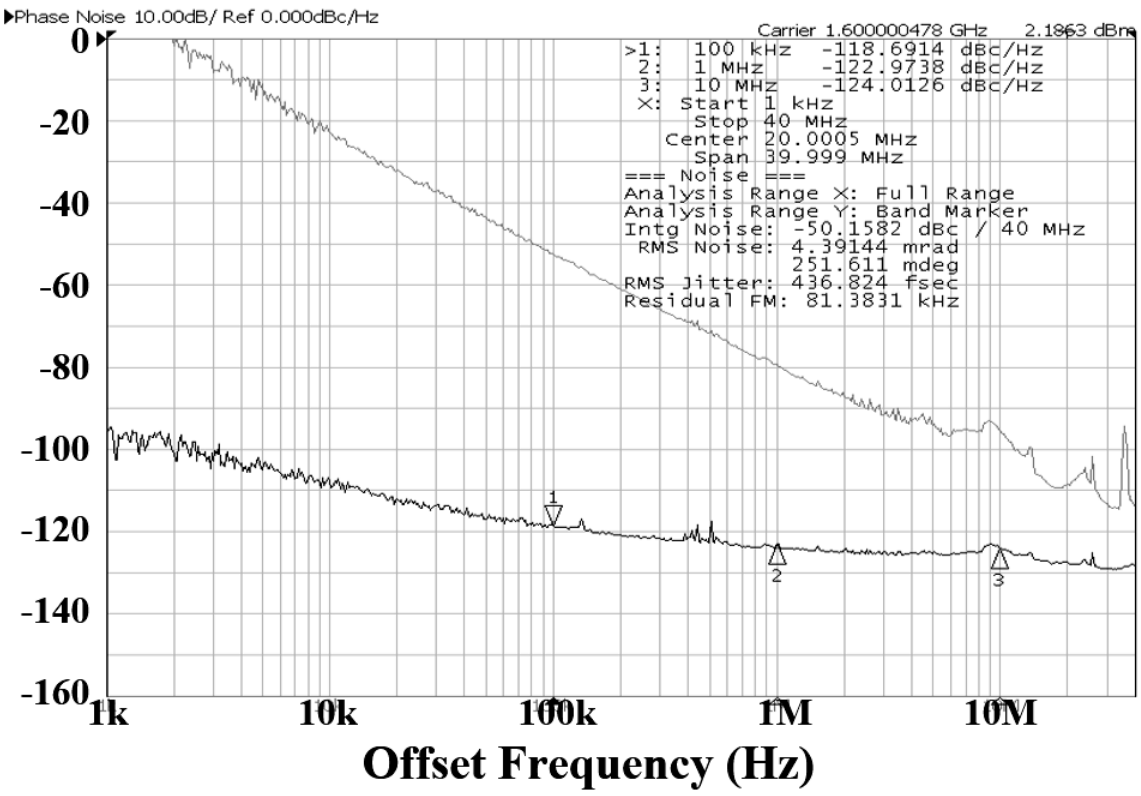
(a)

	Area (mm^2)	Power (mW)
Total	0.0315	3.6
VCO	0.0007	1.1
VCDL	0.0035	1.1
PD/CP	0.0060	0.5
LF	0.0058	NA
Pulse Gen.	0.0002	0.1
Injec. Logic	0.0068	0.8

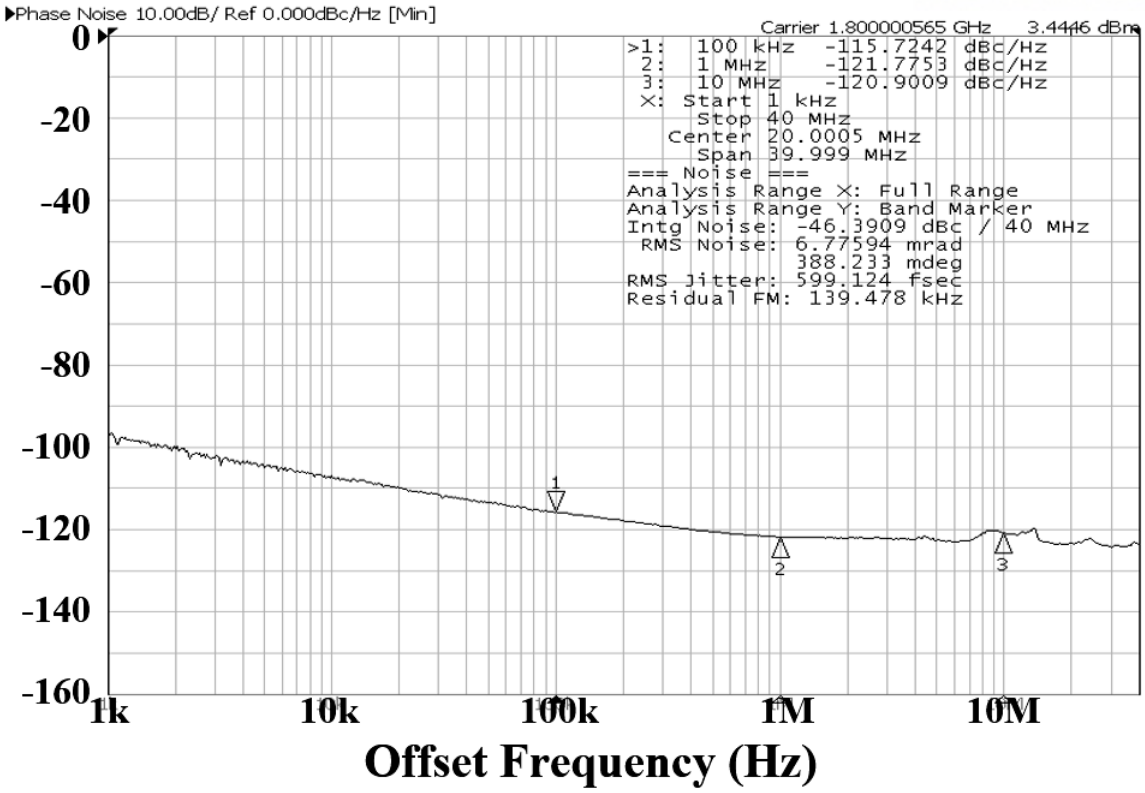
(b)

Figure 34. (a) Microphotograph of the proposed ILCM. (b) Area and power breakdowns.

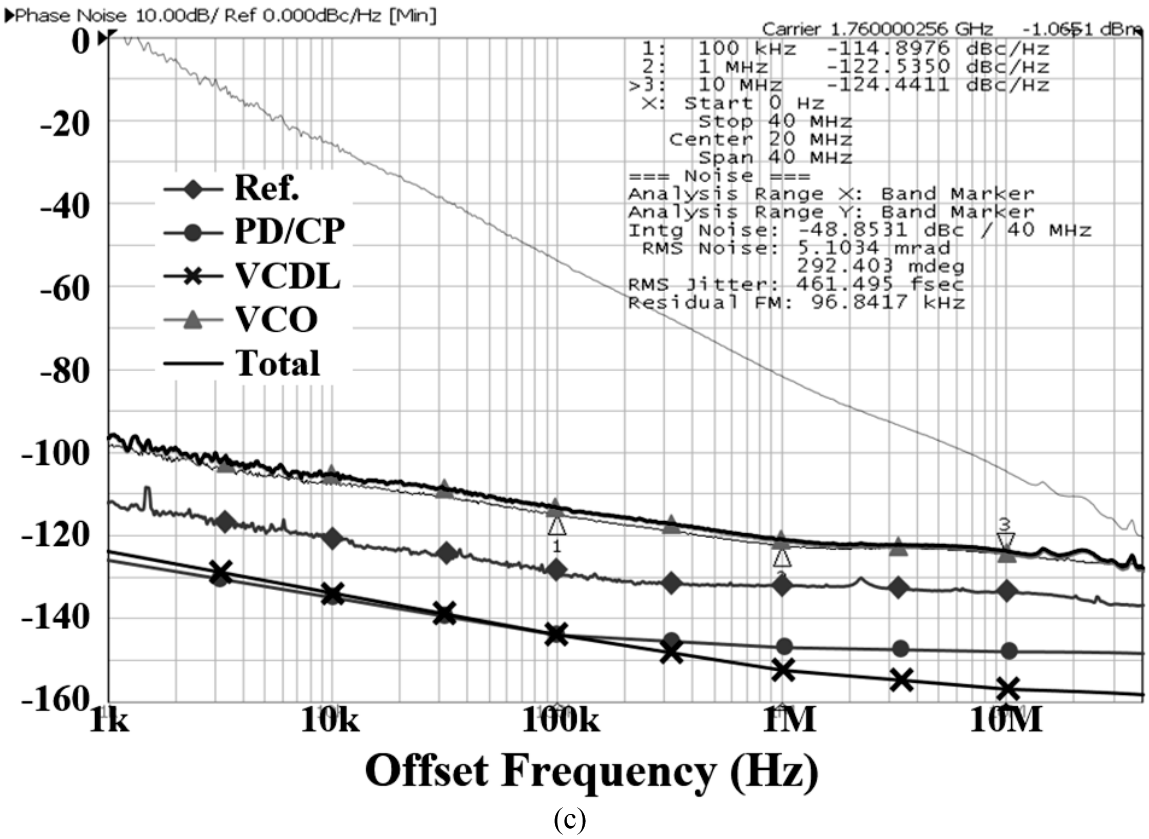
Figure 35 shows phase noise, measured using a signal source analyser, Agilent E5052B. Figure 35(a) shows the phase noise of the output signal with a 1.60-GHz frequency (M = 4.0). Without injection, the spot noise of the free-running VCO was –52.8, –79.1, and –95.7 dBc/Hz at the 100 kHz, 1 MHz, and 10 MHz offsets, respectively. However, when injection-locked, it showed a dramatic improvement in phase noise; thus, spot noise at the same offsets were reduced to –118.7, –123.0, and –124.0 dBc/Hz, respectively. When the integration range is from 1 kHz to 40 MHz (40 MHz was the maximum offset, allowed by the equipment), the RMS-jitter was 437 fs. Figure 35(b) and (c) also show the dramatic improvements in phase noise when output frequencies were 1.80 GHz (M = 4.5) and 1.76 GHz (M = 4.4), respectively. Figure 35(c) compares the measured phase noise and the estimated phase noise based on the noise model (β = 0.85) in Section IV. When the measurement data of the free-running VCO and the reference clock and the simulation data of the other building blocks were used, the overall phase noise curve, plotted by the MATLAB, was in good agreement with the measurement result.



(a)



(b)

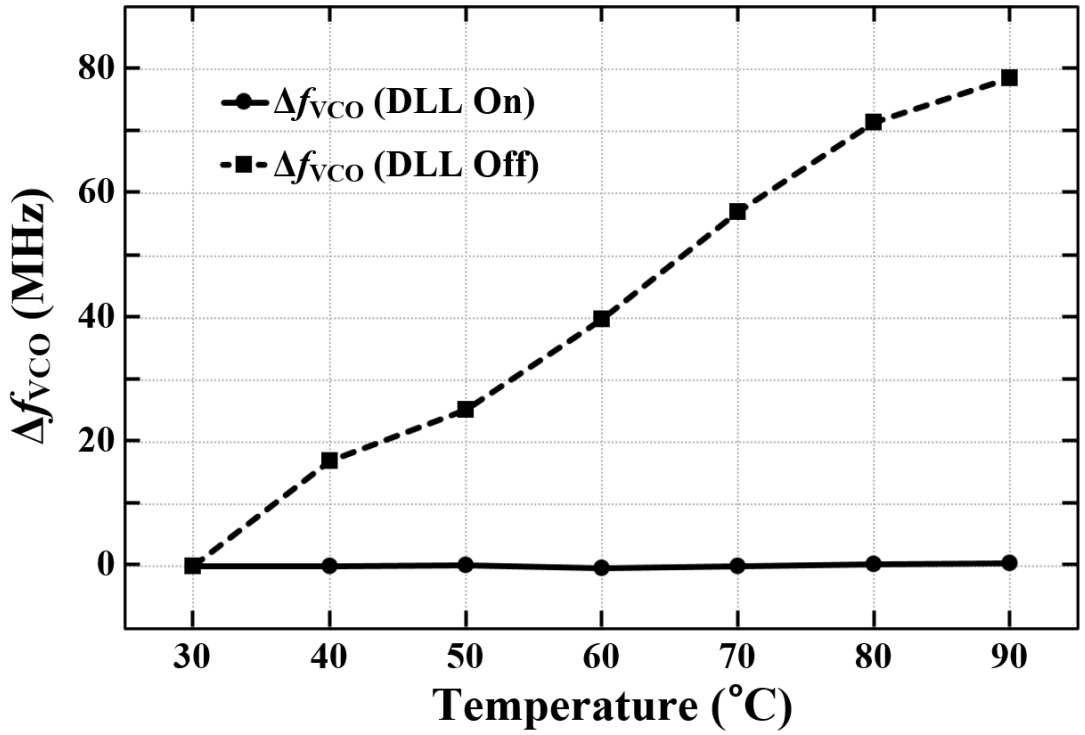


(c)

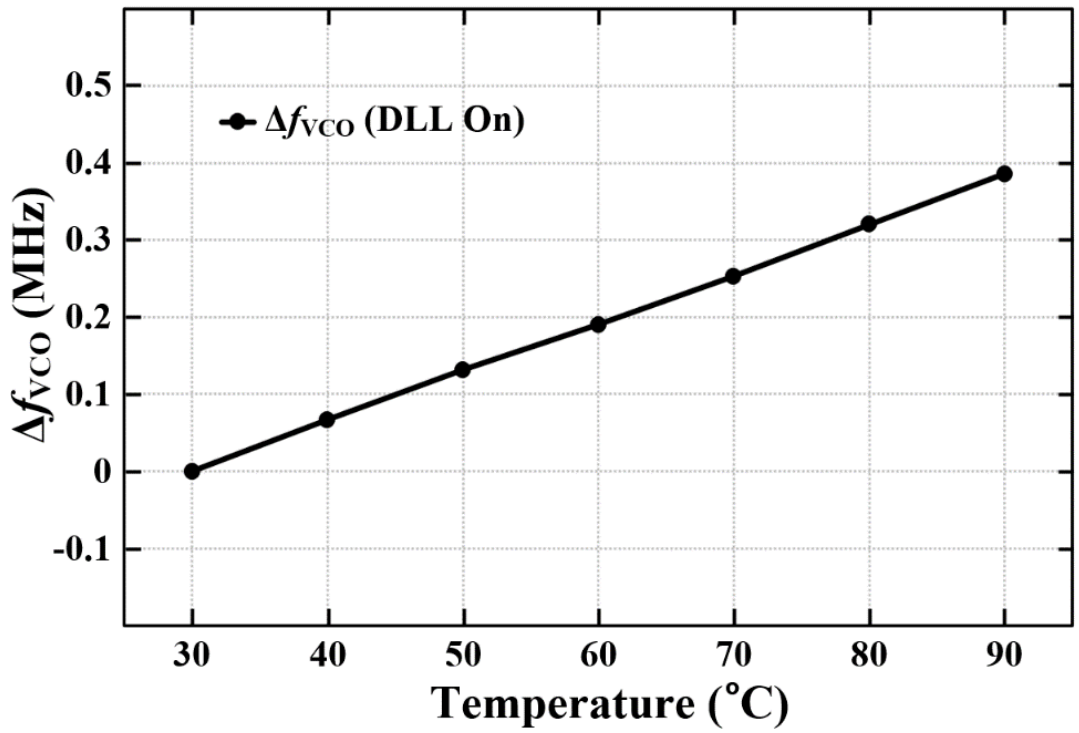
Figure 35. Measured phase noise of the output signal with the frequency of (a) 1.60 GHz (M = 4.0); (b) 1.80 GHz (M = 4.5); and (c) 1.76 GHz (M = 4.4).

Figure 36(a) shows the performance of the proposed DLL-based real-time PVT-calibrator by comparing the variations of the free-running frequency of the VCO, Δf_{VCO}, when the calibrator was off and on as the temperature changes. In this experiment, the pulse generator was disabled (no injection), and the frequency of the VCO was calibrated by the calibrator at 30 ℃ during the initial stage. Then, the calibrator was turned off in the first measurement and kept on in the second measurement while the temperature was swept. When the DLL was turned off, the frequency of the VCO deviated from the initial value by 80 MHz as the temperature increased to 90 ℃. However, when the DLL was kept on, the frequency of the VCO remained near the initial value as the calibrator was adjusting it continuously, and thus, the maximum variation was less than 0.5 MHz, as shown in the Figure 36(b). Figure 36(c) compares the variations of the phase noise and the jitter as the temperature changes with the calibrator off and with it on, while the pulse generator was enabled. The phase noise was measured at the 1-MHz offset, and the jitter was integrated from 1 kHz to 40 MHz. When the calibrator was off, the phase noise and the jitter were degraded sharply as the temperature increased, because the free-running frequency of the VCO drifted away from the target frequency. However, when the calibrator was kept on, the degradations of the phase noise and the jitter were well regulated and restricted to less than 0.5 dB and 8%, respectively.

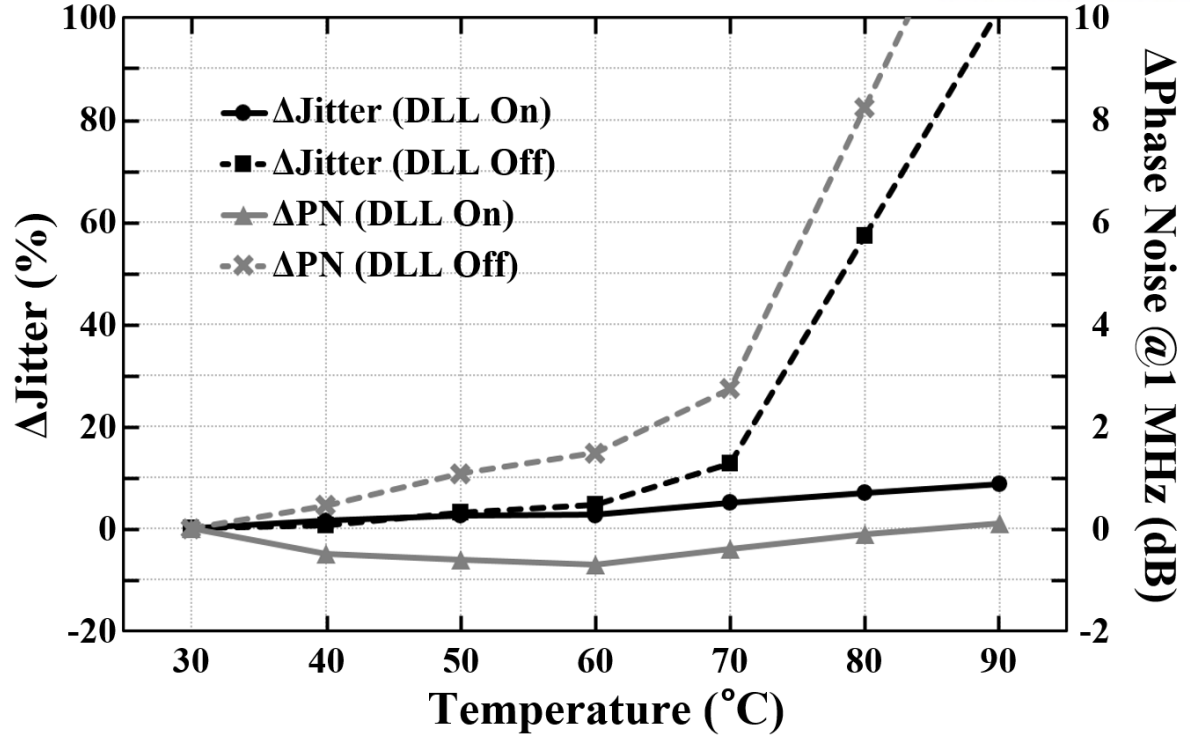
Figure 37(a) – (c) show the performance of the proposed calibrator over the variation of the supply voltage. The procedures of the experiments followed those in the previous experiments, but the supply voltage was swept after the VCO frequency was calibrated at the nominal supply voltage of 1.2 V. When the DLL was turned off, it drifted within ±80 MHz as shown in Figure 37(a), while the VCO frequency stayed close to the initial value when the DLL was kept on, i.e., the variation was less than ± 0.1 MHz as shown in the Figure 37(b). As shown in Figure 37(c), the proposed calibrator restricted the degradations of the phase noise and the jitter over the variation of the supply voltage to less than 0.7 dB and 20%, respectively. Since the phase noise of the ring-VCO itself increased as the supply voltage decreased, the overall phase noise of the ILCM was degraded slightly even though the calibrator was tightly correcting the VCO frequency.



(a)

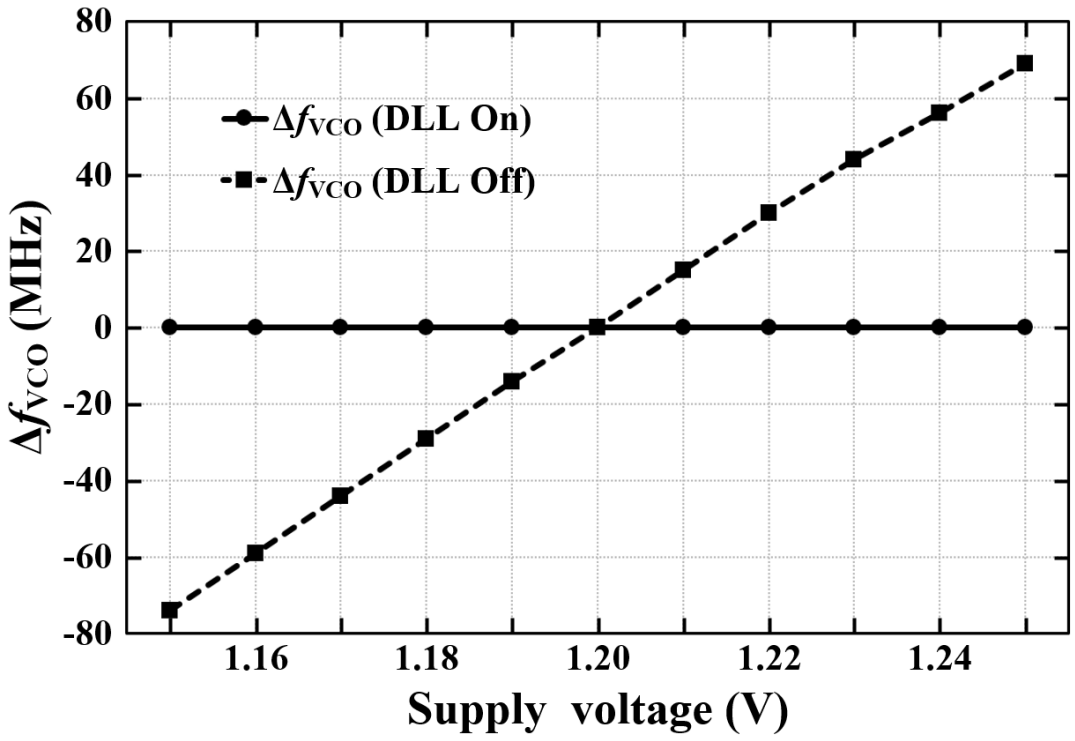


(b)

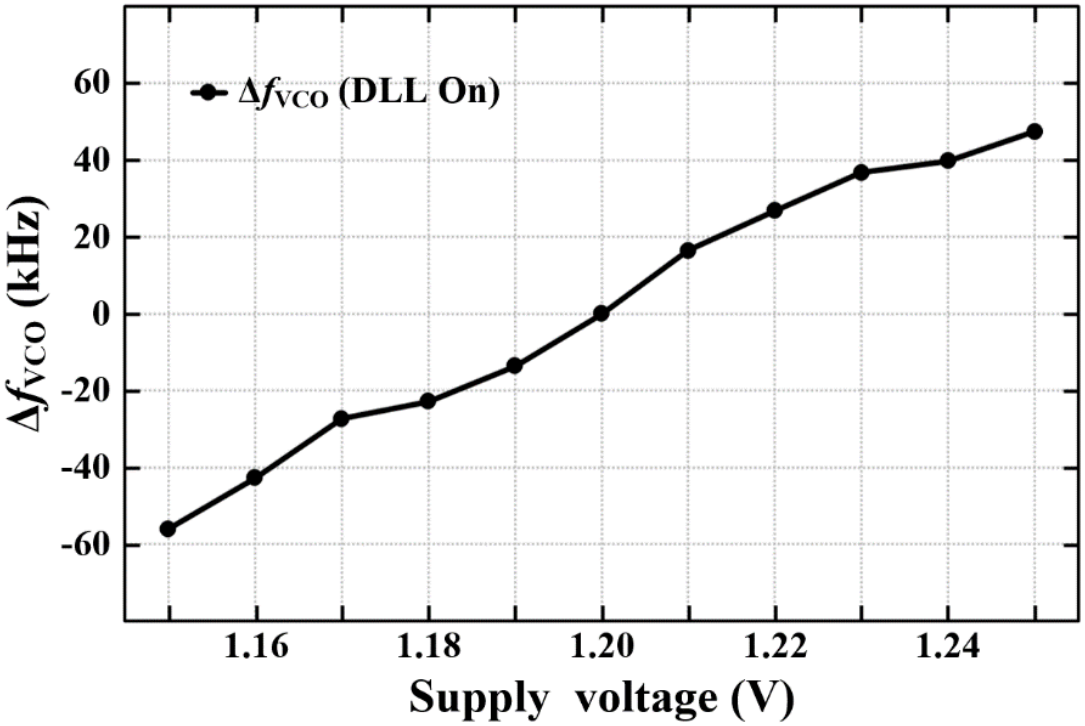


(c)

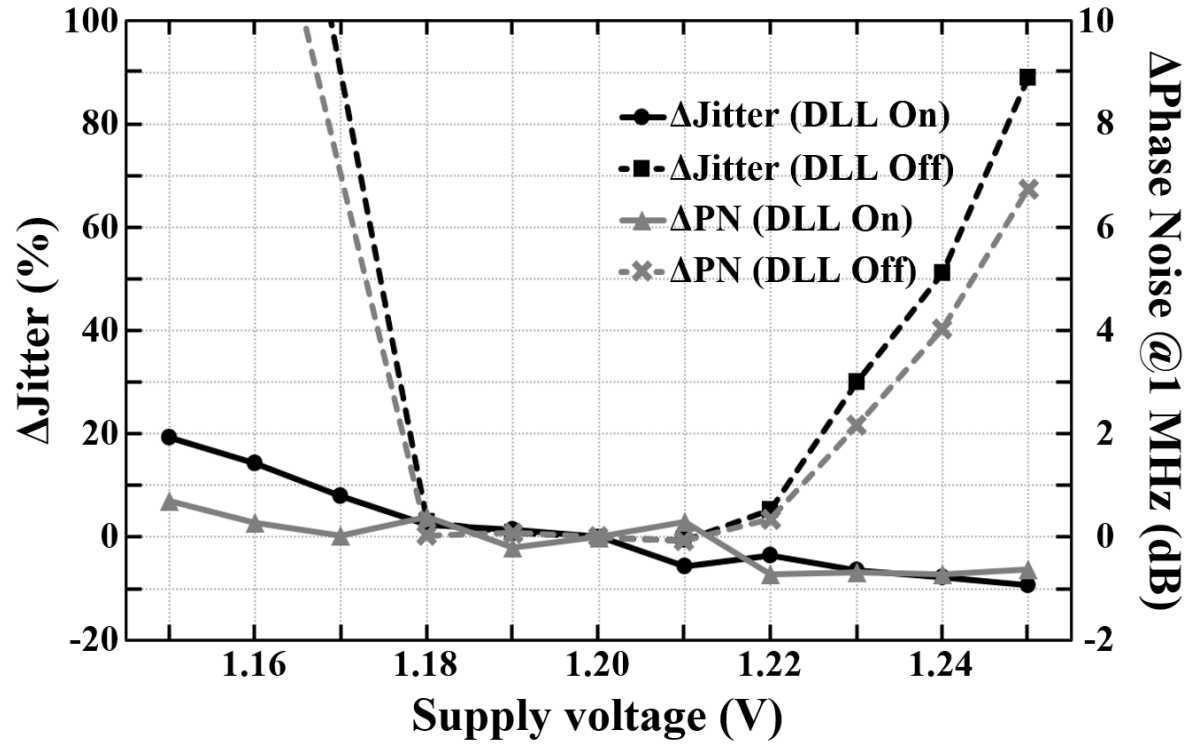
Figure 36. Over temperatures. (a) – (b) Deviation of f_{VCO} from the target frequency. (c) Variations of integrated jitter and phase noise.



(a)



(b)



(c)

Figure 37. Over supply voltages. (a) – (b) Deviation of f_{VCO} from the target frequency. (c) Variations of integrated jitter and phase noise.

Figure 38 shows the level of the spur, which was measured using a spectrum analyser, Agilent N9030A. The level of the spur was –42.8 dBc at the 80-MHz offset from the 1.36-GHz output frequency. When the power of the spur was included in the jitter calculation, the integrated jitter was approximately 1.2 ps [23].

Figure 39 shows the frequency-switching time of the calibrator when the target frequency changed from 1.92 to 1.76 GHz. Based on a DLL, the proposed calibrator can switch the VCO frequency more rapidly than conventional calibrators. While the injection was disabled to measure the lock time of the DLL, the frequency deviations from target frequencies were less than 1%.

Table 3 compares the performance of the proposed ILCM with state-of-the-art ring-VCO clock multipliers based on the injection-locking. The proposed ILCM achieved both capabilities of a fractional resolution and a real-time PVT-calibration, and shows a lower jitter and a better figure-of-merit (FoM) than other fractional-resolution architectures. Using a simple architecture of a DLL-based calibrator, the proposed ILCM occupied a small silicon area, and reduced the frequency-switching time.

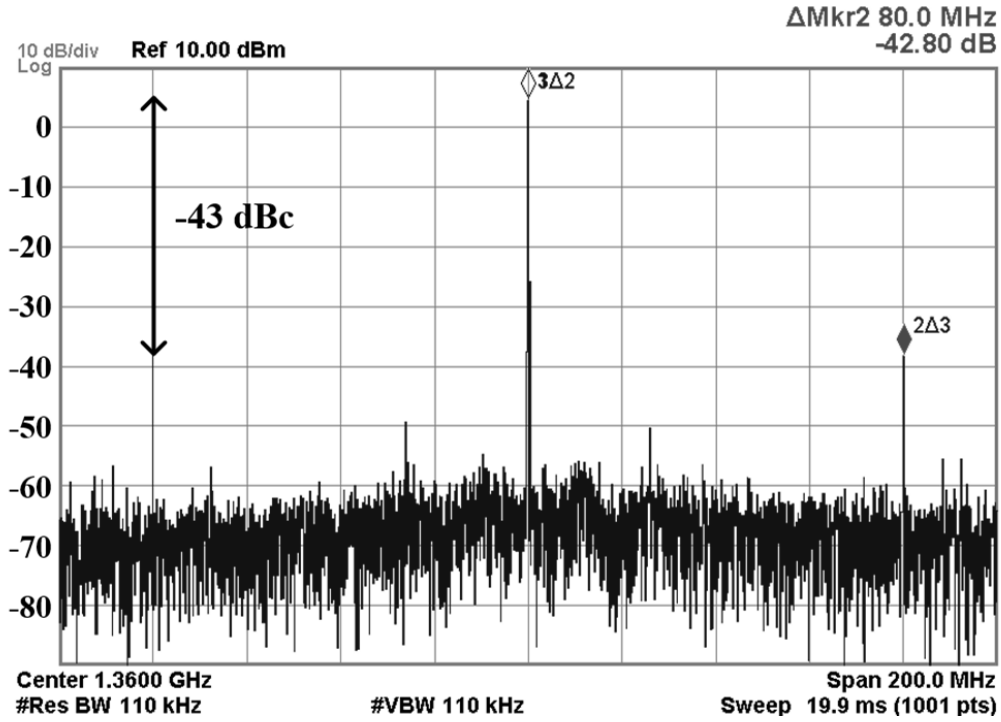


Figure 38. Measured spectrum of the output signal with the frequency of 1.36 GHz (M = 3.4).

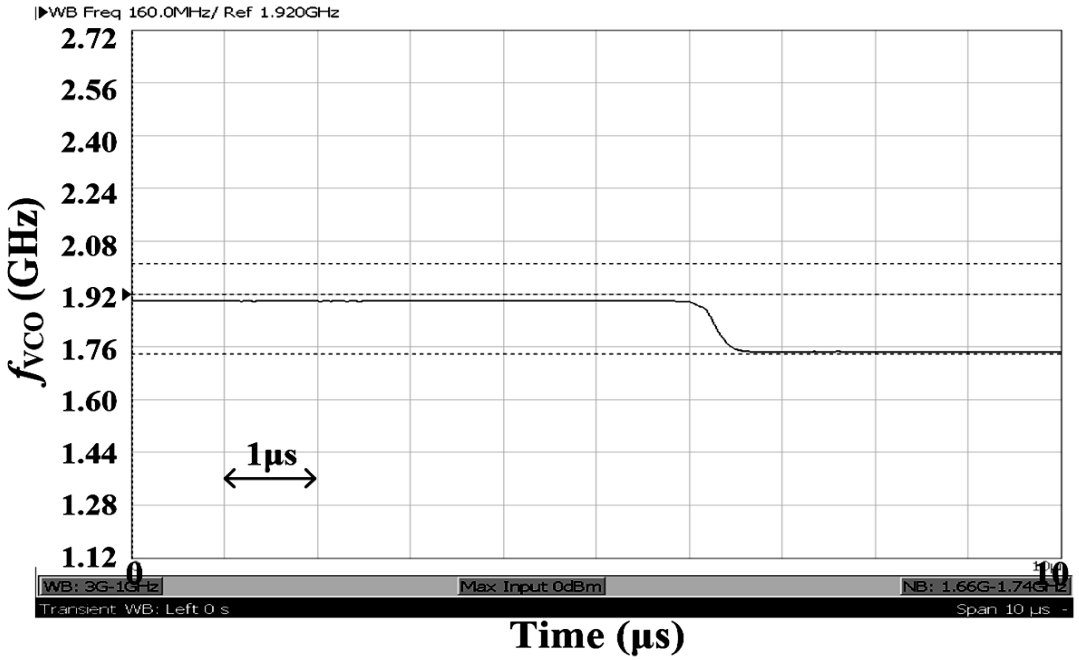


Figure 39. Measured frequency-switching time of the DLL, when the target frequency changed from 1.92 to 1.76 GHz (no injection).

Table 3. Performance comparison with state-of-the-art ring-type ILCMs

	[7]	[9]	[13]	[15]	This work
Process	20 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Topology	IL + PPM	IL + PLL	IL + Dual loop	IL + Dual loop	IL + DLL
Output Freq. (f_O)	15 GHz	576 – 608 MHz	0.5 – 1.6 GHz	0.4 – 1.4 GHz	1.2 – 2.0 GHz
Reference Freq.	1875 MHz	32 MHz	300 MHz	150 MHz	400 MHz
Frac. Resolution	N	Y	N	N	Y
Real-time Calibration	N	N	Y	Y	Y
Freq. Resolution	f_{REF}	$f_{REF}/32$	f_{REF}	f_{REF}	$f_{REF}/10$
1-MHz PN @ f_O	–115 dBc/Hz @ 15GHz	–114 dBc/Hz @ 580 MHz	–128 dBc/Hz @ 1.2 GHz	–115 dBc/Hz @ 0.9 GHz	–122.9 dBc/Hz @ 1.6 GHz
Integ. Jitter (σ_t) (Integ. Range)	268 fs (100k – 1 GHz)	2.45 ps (100 – 40 MHz)	0.7 ps (10k – 40 MHz)	1.7 ps (10k – 40 MHz)	440 fs (1k – 40 MHz)
Spur	–48 dBc	–60 dBc	–57 dBc	–41 dBc	–43 dBc
Power Cons. (P_{DC})	46.2 mW	10.5 mW	0.97 mW	0.78 mW	3.6 mW
Active area	0.044 mm^2	0.158 mm^2	0.022 mm^2	0.0066 mm^2	0.032 mm^2
Freq. Calibration Time	NA	NA	NA	NA	< 500 ns
FoM	–234.8 dB	–222.0 dB	–243.2 dB	–236.4 dB	–241.6 dB

***** FoM: $10 \cdot \log10(\sigma_t^2 \cdot P_{DC})$ dB

VI. Conclusions

In this thesis, a dual-loop ILCM using a two-phase PVT-calibrator for a ΔΣ PLL, and a fractional-resolution ILCM using a DLL-based PVT-calibrator were presented. Both architectures were based on injection-locking; thus, they required the small silicon area and a low power budget.

The proposed dual-loop ILCM using the two-phase PVT-calibrator, reduced the frequency-switching time as well as tightly regulating the phase noise degradation by switching the calibration resolution according to the phase. Due to the real-time PVT-calibration of the proposed ILCM, the degradation of the phase noise over the temperature was regulated to less than 0.5 dB at the 1 MHz offset. In addition, the ILCM can generate five different output frequencies, 19.2, 28.8, 48.0, 57.6, and 96.0 MHz with a 19.2 MHz external clock in a programmable fashion. The measurements of the prototype-PLL showed that high-frequency reference clocks from the proposed ILCM, effectively improved the phase noise performance.

The proposed fractional-resolution ILCM using a DLL-based calibrator achieved a resolution that was 10% of the reference frequency by rotationally switching the injection-point of the multi-stage ring-VCO. The ring-VCO and the DLL consist of identical delay cells, and share the same control voltage; thus, the VCO frequency can be tuned at near a target frequency, a non-integer times the reference frequency, by changing the ratio between the numbers of the stages of the VCDL and the VCO. In addition, due to the calibrator based on a DLL, the proposed ILCM obtained a short frequency-switching time. In common with the dual-loop ILCM, the injection-locked VCO can overcome real-time frequency drifts as well as static process variations. Therefore, the proposed DLL-based PVT-calibrator restricted the degradations of phase noise and jitter over the temperature and the supply variations to less than 0.7 dB and 20%, respectively.

In both architectures, the ILCMs are free from the timing issue of conventional PLL-based architectures, since the VCO is not enclosed by a loop.

REFERENCES

[1] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, p. 1415–1424, Sep. 2004.

[2] S. Ye, L. Jansson and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2002.

[3] S. Ye, L. Jansson and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, p. 1795–1803, Dec. 2002.

[4] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, p. 1539–1553, May 2009.

[5] E. Monaco, M. Pozzoni, F. Svelto and A. Mazzanti, "Injection-locked CMOS frequency doublers for μ-wave and mm-wave applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, p. 1565–1574, Aug. 2010.

[6] S. Lee, L. Wang and Y. Lin, "A CMOS quadrature VCO with subharmonic and injection-locked techniques," *IEEE Transactions on Circuits and Systems II: Exp. Briefs*, vol. 57, no. 11, p. 843–847, Nov. 2010.

[7] J. Chien, P. Upadhyaya, H. Jung, S. Chen, W. Fang, A. Niknejad, J. Savoj and K. Chang, "A pulse-position-modulation phase-noise-reduction technique for a 2-to-16GHz injection-locked ring oscillator in 20nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014.

[8] Y. Huang and S. Liu, "A 2.4-GHz subharmonically injection-locked PLL with self-calibrated injection timing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, p. 417–428, Feb. 2013.

[9] P. Park, J. Park, H. Park and S. Cho, "An all-digital clock generator using a fractionally injection-locked oscillator in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012.

[10] S. Lee, S. Ikeda, H. Ito, S. Tanoi, N. Ishihara and K. Masu, "An inductorless injection-locked PLL with 1/2- and 1/4-integral subharmonic locking in 90 nm CMOS," in *IEEE RFIC Dig.*, Jun. 2012.

[11] B. Helal, C. Hsu, K. Johnson and M. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, p. 1391–1400, May 2009.

[12] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada and A. Matsuzawa, "A 0.022 mm2 970μW injection-locked PLL with -243 dB FOM using synthesizable all-digital PVT calibration circuits," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013.

[13] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada and A. Matsuzawa, "A compact, low-power and low-jitter dual-loop Injection locked PLL using all-digital PVT calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, p. 50–60, Jan. 2014.

[14] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada and A. Matsuzawa, "A 0.0066mm2 780μW fully synthesizable PLL with a current-output DAC and an interpolative phase-coupled oscillator using edge-injection technique," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014.

[15] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada and A. Matsuzawa, "A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, p. 68–80, Jan. 2015.

[16] C. Liang and K. Hsiao, "An injection-locked ring PLL with self-aligned injection window," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011.

[17] I. Lee, Y. Chen, S. Liu, C. Jou, F. Hsueh and H. Hsieh, "A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013.

[18] M. Izad and C. Heng, "A pulse shaping technique for spur suppression in injection-locked synthesizers," *IEEE J. Solid-State Circuits*, vol. vol. 47, no. no. 3, p. 652–664, Mar. 2012.

[19] Y. Lee, M. Kim, T. Seong and J. Choi, "A low phase noise injection-locked programmable reference clock multiplier with a two-phase PVT-calibrator for ΣΔ PLLs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, p. 635–644, March 2015.

[20] M. Kim, S. Choi and J. Choi, "A 450-fs Jitter PVT robust fractional-resolution injection-locked clock multiplier using a DLL-based calibrator with replica-delay-cells," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2015.

[21] F. Liao and S. Lu, "A waveform-dependent phase-noise analysis for edge-combining DLL frequency multipliers," *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 4, p. 1086–1096, Apr. 2012.

[22] C. Vaucher, Architectures for RF Frequency Synthesizers, Boston, MA: Kluwer, 2002.

[23] M. P. Li, Jitter, Noise, and Signal Integrity at High-Speed, Englewood Cliffs, NJ: Prentice-Hall, 2007.

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